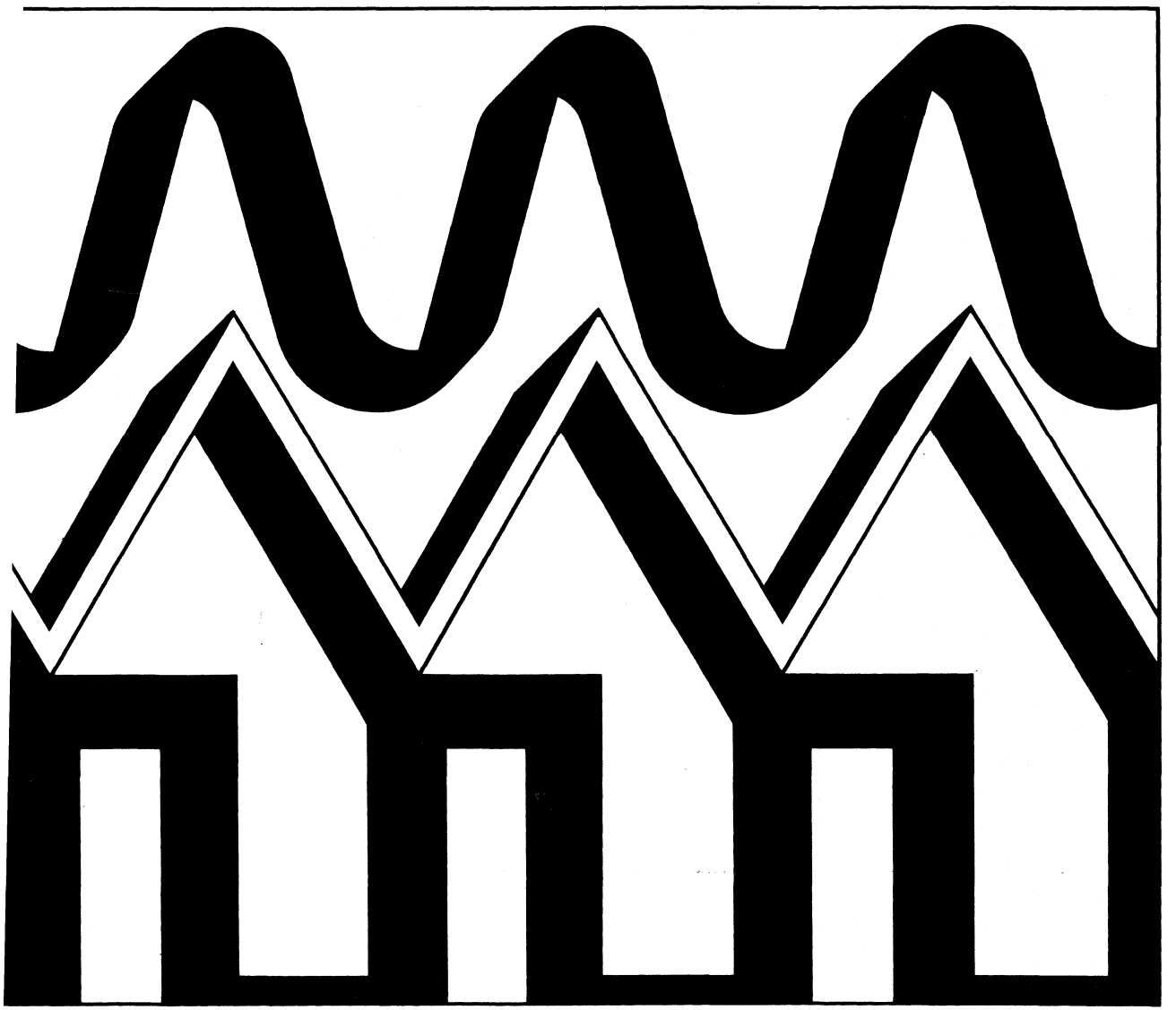
Intersil

Analog Products Catalog

VOLUME II



Introduction

Volume II of Intersil's Analog Products Catalog contains devices most recently introduced and recommended for new designs. These products have not previously been published in any Intersil catalog.

Note that Volume II does not contain the entire Intersil Analog Production Line. For the complete line, refer to the Product Line Listing, page iii of this catalog.

Further information on older Intersil analog products can be found in the Analog Products Catalog, Volume I.

Functional Index to Volume II

Product Line Listing

A complete listing of the Intersil Analog Products line. Detailed specifications can be found in the Data Sections of Volumes I and II, as indicated here.

Data Section

HIGH SLEW RATE OPERATIONAL AMPLIFIERS

2500 2520
2502 2522
2505 2525

FEATURES

- Slew Rate – Up to 120 V/μs
- Settling Time – 200 ns to 0.1%
- Bias Current – 100 nA
- Gain Bandwidth Product – 30 MHz
- Internal Frequency Compensation
- Radiation Hardened
- Meets MIL-STD-883

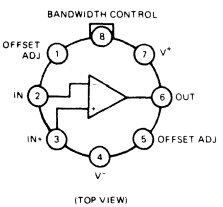
GENERAL DESCRIPTION

The 2500 series of high slew rate operational amplifiers are monolithic integrated circuits fabricated using dielectric isolation and thin film resistors. These internally compensated amplifiers feature excellent input parameters, high gain and wide bandwidth. They are ideally suited for D/A and A/D converter circuits, pulse amplifiers and high frequency buffer amplifiers.

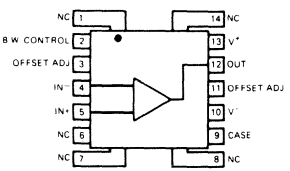
2500 through 2515 are compensated for unity gain. 2520 through 2525 are intended for closed loop gains of 3 or greater, and feature increased slew rates and gain-bandwidth products.

CONNECTION DIAGRAMS

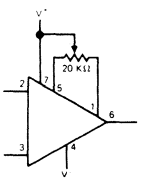
TO-99



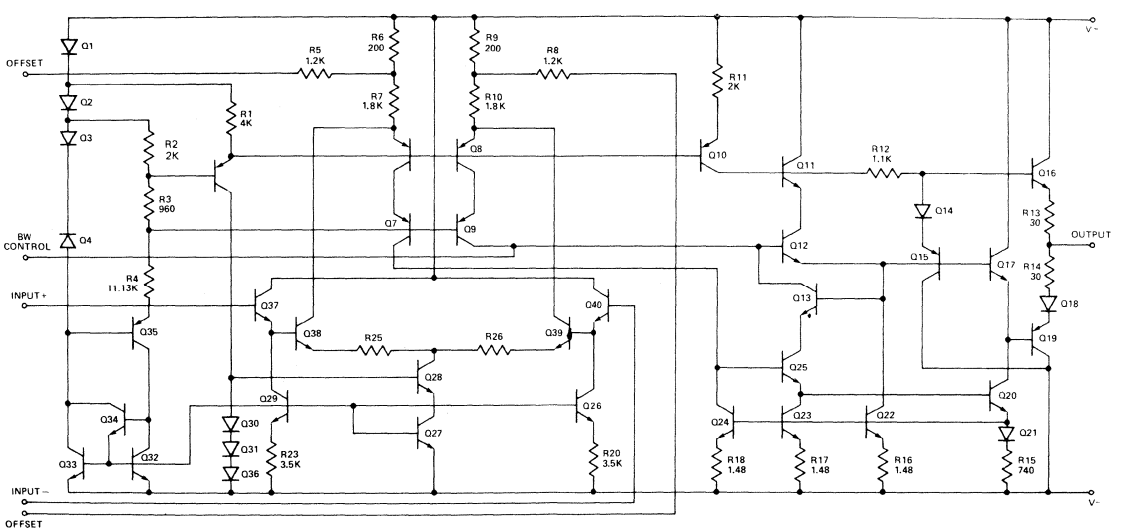
TO-86 Flat Pack



VOLTAGE OFFSET NULL CIRCUIT



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

2500
2502
2505

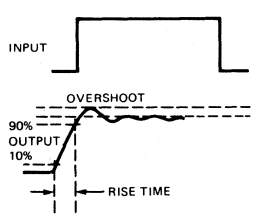
Supply Voltage	±20V
Input Voltage (Note 1)	±15V
Differential Input Voltage	±15V
Peak Output Current	±50 mA
Internal Power Dissipation (Note 2)	300 mW
Lead Temperature (Soldering, 60 sec)	300°C
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C (2500, 2502) 0°C to +75°C (2505)

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±15V unless otherwise specified)

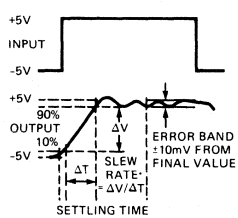
PARAMETER	CONDITIONS	2500			2502			2505			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10\ k\Omega$		2	5		4	8		4	8	mV
Input Offset Current			10	25		20	50		20	50	nA
Input Resistance		25	50		20	50		20	50		MΩ
Large Signal Voltage Gain	R_L = 2kΩ, V_O = ±10V	20K	30k		15k	25k		15k	25k		V/V
Gain Bandwidth	$A_V > 10$		12			12			12		MHz
Full Power Bandwidth	R_L = 2 kΩ, C_L = 50 pF, V_O = $20V_{p-p}$	350	500		300	500		300	500		kHz
Rise Time (Notes 3, 4)	R_L = 2 kΩ, C_L = 50 pF		25	50		25	50		25	50	ns
Overshoot (Notes 3, 4)	R_L = 2 kΩ, C_L = 50 pF		25	40		25	50		25	50	%
Slew Rate (Note 3)	R_L = 2 kΩ, C_L = 50 pF, V_O = ±10V	±25	±30		±20	±30		±20	±30		V/μs
Settling Time (to 0.1% of Final Value) (Note 3)	R_L = 2 kΩ, C_L = 50 pF, V_O = ±10V		330			330			330		ns
Output Current	V_O = ±10V	±10			±10			±10			mA
Supply Current			4	6		4	6		4	6	mA
THE FOLLOWING SPECIFICATIONS APPLY FOR OPERATING TEMPERATURE RANGE											
Input Offset Voltage	$R_S \leq 10\ k\Omega$			8			10			10	mV
Input Offset Current				50			100			100	nA
Input Bias Current	+25°C to +125°C		100	200		125	250				nA
	-55°C to +25°C		200	400		250	500				nA
	+25°C to +75°C								125	250	nA
	0°C to +25°C								250	500	nA
Offset Voltage Average Drift	$R_S \leq 10\ k\Omega$		20			20			20		μV/°C
Offset Current Average Drift			0.1			0.1			0.1		nA/°C
Common Mode Rejection Ratio	V_{CM} = ±5V	80	90		74	90		74	90		dB
Common Mode Range		±10			±10			±10			V
Supply Voltage Rejection Ratio	ΔV = ±5V	80	90		74	90		74	90		dB
Large Signal Voltage Gain	R_L = 2 kΩ, V_O = ±10V	15k			10k			10k			V/V
Output Voltage Swing	R_L = 2 kΩ	±10	±12		±10	±12		±10	±12		V

NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
NOTE 2: Derate TO-86 at 4.5 mW/°C above 84°C; derate TO-99 at 6.6 mW/°C above 105°C.
NOTE 3: A_V = 1.
NOTE 4: V_O = 400 mV_{p-p}.

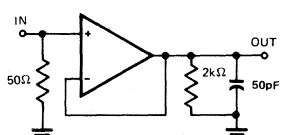
TRANSIENT RESPONSE



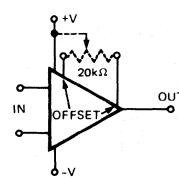
SLEW RATE AND SETTLING TIME



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

ABSOLUTE MAXIMUM RATINGS

2520
2522
2525

Supply Voltage	±20V
Input Voltage (Note 1)	±15V
Differential Input Voltage	±15V
Peak Output Current	±50 mA
Internal Power Dissipation (Note 2)	300 mW
Lead Temperature (Soldering, 60 sec)	300°C
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C (2520, 2522) 0°C to +75°C (2525)

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±15V unless otherwise specified)

PARAMETER	CONDITIONS	2520			2522			2525			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10\ k\Omega$		4	8		5	10		5	10	mV
Input Offset Current			10	25		20	50		20	50	nA
Input Resistance		50	100		40	100		40	100		MΩ
Large Signal Voltage Gain	R_L = 2 kΩ, V_O = ±10V	10k	15k		7.5k	15k		7.5k	15k		V/V
Gain Bandwidth	$A_V > 10$		30			30			30		MHz
Full Power Bandwidth	R_L = 2 kΩ, C_L = 50 pF, V_O = 20Vp-p	1500	2000		1200	1600		1200	1600		kHz
Rise Time (Notes 3,4)	R_L = 2 kΩ, C_L = 50 pF		15	50		15	50		15	50	ns
Overshoot (Notes 3, 4)	R_L = 2 kΩ, C_L = 50 pF										%
Slew Rate (Note 3)	R_L = 2 kΩ, C_L = 50 pF, V_O = ±10V	±100	±120		±80	±120		±80	±120		V/μs
Settling Time (to 0.1% of Final Value) (Note 3)	R_L = 2 kΩ, C_L = 50 pF, V_O = ±10V		200			200			200		ns
Output Current	V_O = ±10V	±10			±10			±10			mA
Supply Current			4	6		4	6		4	6	mA
THE FOLLOWING SPECIFICATIONS APPLY FOR OPERATING TEMPERATURE RANGE											
Input Offset Voltage	$R_S \leq 10\ k\Omega$			11			14			14	mV
Input Offset Current				50			100			100	nA
Input Bias Current	+25°C to +125°C		100	200		125	250				nA
	-55°C to +25°C		200	400		250	500				nA
	+25°C to +125°C								125	250	nA
	-55°C to +25°C								250	500	nA
Offset Voltage Average Drift	$R_S \leq 10\ k\Omega$		20			30			30		μV/°C
Offset Current Average Drift			0.1			0.1			0.1		nA/°C
Common Mode Rejection Ratio	V_{CM} = ±5V	80	90		74	90		74	90		dB
Common Mode Range		±10			±10			±10			V
Supply Voltage Rejection Ratio	ΔV = ±15	80	90		74	90		74	90		dB
Large Signal Voltage Gain	R_L = 2 kΩ, V_O = ±10V	7.5k			5k			5k			V/V
Output Voltage Swing	R_L = 2 kΩ	±10	±12		±10	±12		±10	±12		V

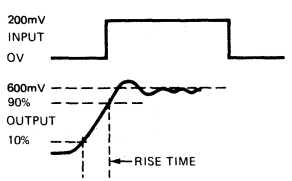
NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 2: Derate TO-86 at 4.5 mW/°C above 84°C; derate TO-99 at 6.6 mW/°C above 105°C.

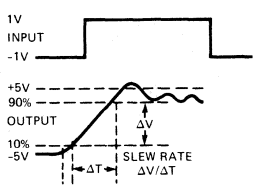
NOTE 3: A_V = 3.

NOTE 4: V_O = 600 mV_{p-p}.

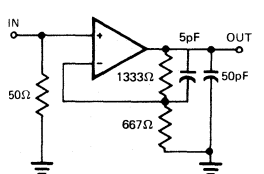
TRANSIENT RESPONSE



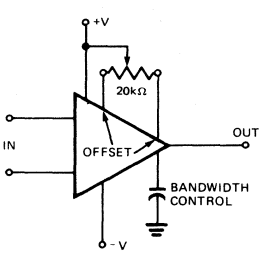
SLEW RATE



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST AND BANDWIDTH CONTROL HOOK-UP



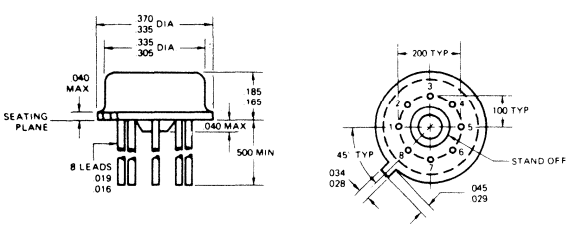
NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBER
2500	-55°C to +125°C	TO-99 Flat Pack	HA2-2500-2 HA9-2500-2
2502	-55°C to +125°C	TO-99 Flat Pack	HA2-2502-2 HA9-2502-2
2505	0°C to +75°C	TO-99 Flat Pack	HA2-2505-5 HA9-2505-5
2520	-55°C to +125°C	TO-99 Flat Pack	HA2-2520-2 HA9-2520-2
2522	-55°C to +125°C	TO-99 Flat Pack	HA2-2522-2 HA9-2522-2
2525	0°C to +75°C	TO-99 Flat Pack	HA2-2525-5 HA9-2525-5

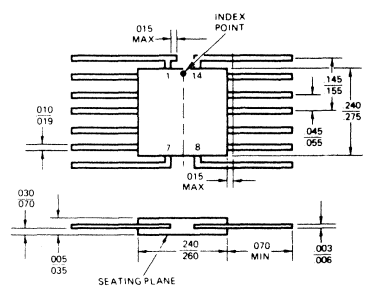
PACKAGE DIMENSIONS

TO-99 Package



NOTES: All dimensions in inches.
Leads are gold-plated Kovar.

TO-86 Flat Pack



EIGHT-BIT/TWELVE-BIT SUCCESSIVE APPROXIMATION REGISTERS

2502
2503
2504

FEATURES

- Contains all the storage and control for successive approximation A-to-D converters.
- Provision for register extension or truncation.
- Can be operated in START-STOP or continuous conversion mode.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Can be used as serial-to-parallel counter or ring counters.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

GENERAL DESCRIPTION

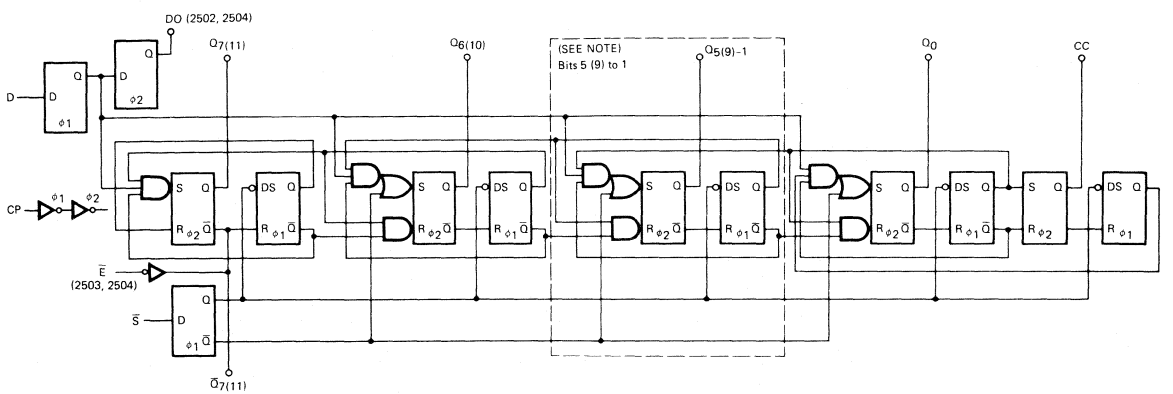
The 2502, 2503 and 2504 are 8-bit and 12-bit TTL Successive Approximation Registers. The registers contain all the digital control and storage necessary for successive approximation analog-to-digital conversion. They can also be used in digital systems as the control and storage element in recursive digital routines.

The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the 2502 and 2504 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration.

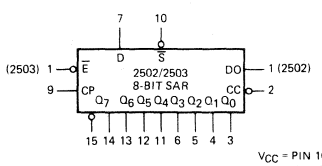
The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state $Q_7(11)$ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting. After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the $Q_7(11)$ register bit and the $Q_6(10)$ register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the $Q_6(10)$ register bit and $Q_5(9)$ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q_0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, on the 2503 and 2504 allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the Start signal resets the register, the $\overline{E}$ signal goes HIGH, forcing the $Q_7(11)$ bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level (Ground). If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the CC signal to indicate the end of conversion.

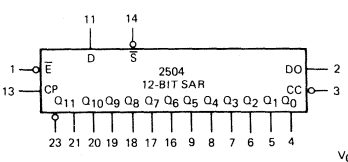
LOGIC DIAGRAM/SYMBOLS



NOTE:
1. CELL LOGIC IS REPEATED FOR REGISTER STAGES. Q_5 TO Q_1 2502/3 Q_9 TO Q_1 2504
2. NUMBERS IN PARENTHESES ARE FOR 2504



V_{CC} = PIN 16
GND = PIN 8



V_{CC} = PIN 16
GND = PIN 12
NC = PINS 10, 15, 22

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground Potential Continuous	-0.5V to +7V
DC Voltage Applied to Outputs for High Output State	-0.5V to +V_{CC} max
DC Input Voltage	-0.5V to +5.5V
Output Current, Into Outputs	30mA
DC Input Current	-30mA to +5.0mA
Temperature (Ambient) Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C

ORDERING INFORMATION

Temperature Range	Package	2502 Order No.	2503 Order No.	2504 Order No.
0 to +75°C	Ceramic DIP	2502CJE	2503CJE	2504CJG
0 to +75°C	Epoxy DIP	2502CPE	2503CPE	2504CPG
0 to +75°C	Dice	2502C/D	2503C/D	2504C/D
-55 to +125°C	Ceramic DIP	2502MJE	2503MJE	2504MJG
-55 to +125°C	Dice	2502M/D	2503M/D	2504M/D

ELECTRICAL CHARACTERISTICS

2502C 2503C 2504C T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
2502M 2503M 2504M T_A = -55°C to +125°C V_{CC} = 5.0V ±10% (unless otherwise noted)

PARAMETERS	DESCRIPTION	TEST CONDITIONS			MIN.	TYP. (Note 1)	MAX.	UNITS
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = -0.48mA V_{IN} = V_{IH} or V_{IL}			2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 9.6mA V_{IN} = V_{IH} or V_{IL}				0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				-1.0	-1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				6.0	40	µA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V			-10	-25	-45	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	2502	M		65	85	mA
				C		65	95	
			2503	M		60	80	mA
				C		60	90	
			2504	M		90	110	mA
				C		90	124	

NOTE 1: Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
NOTE 2: Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

SWITCHING CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF

PARAMETERS	DESCRIPTION		MIN.	TYP.	MAX.	UNITS
t_{pd+}	Turn Off Delay CP to Output HIGH		10	26	38	ns
t_{pd-}	Turn On Delay CP to Output LOW		10	18	28	ns
t_s(D)	Set-up Time Data Input		-10	4	8	ns
t_s(S)	Set-up Time Start Input		0	9	16	ns
t_{pd+}(E)	Turn Off Delay E to Q_7(11) HIGH	(2503/4) C_P = H, $\overline{S}$ = L		13	19	ns
t_{pd-}(E)	Turn On Delay E to Q_7(11) LOW			16	24	ns
t_{pwL}(CP)	Minimum LOW Clock Pulse Width			28	46	ns
t_{pwH}(CP)	Minimum HIGH Clock Pulse Width			12	20	ns
f_{max}	Maximum Clock Frequency		15	25		MHz

2502/3 LOADING RULES (IN UNIT LOADS)

INPUT/ OUTPUT	PIN NO.'s	INPUT UNIT LOAD LOW	INPUT UNIT LOAD HIGH	FANOUT OUTPUT HIGH	FANOUT OUTPUT LOW
$\overline{E}$ (2503)	1	2	2	–	–
DO (2502)	1	–	–	12	6
$\overline{CC}$	2	–	–	12	6
Q_0	3	–	–	12	6
Q_1	4	–	–	12	6
Q_2	5	–	–	12	6
Q_3	6	–	–	12	6
D	7	2	2	–	–
GND	8	–	–	–	–
CP	9	1	1	–	–
$\overline{S}$	10	1	2	–	–
Q_4	11	–	–	12	6
Q_5	12	–	–	12	6
Q_6	13	–	–	12	6
$\overline{Q_7}$	14	–	–	12	6
Q_7	15	–	–	12	6
V_{CC}	16	–	–	–	–

2504 LOADING RULES (IN UNIT LOADS)

INPUT/ OUTPUT	PIN NO.'s	INPUT UNIT LOAD LOW	INPUT UNIT LOAD HIGH	FANOUT OUTPUT HIGH	FANOUT OUTPUT LOW
$\overline{E}$	1	2	2	–	–
DO	2	–	–	12	6
$\overline{CC}$	3	–	–	12	6
Q_0	4	–	–	12	6
Q_1	5	–	–	12	6
Q_2	6	–	–	12	6
Q_3	7	–	–	12	6
Q_4	8	–	–	12	6
Q_5	9	–	–	12	6
NC	10	–	–	–	–
D	11	2	2	–	–
GND	12	–	–	–	–
CP	13	1	1	–	–
$\overline{S}$	14	1	2	–	–
NC	15	–	–	–	–
Q_6	16	–	–	12	6
Q_7	17	–	–	12	6
Q_8	18	–	–	12	6
Q_9	19	–	–	12	6
Q_{10}	20	–	–	12	6
$\overline{Q_{11}}$	21	–	–	12	6
NC	22	–	–	–	–
Q_{11}	23	–	–	12	6
V_{CC}	24	–	–	–	–

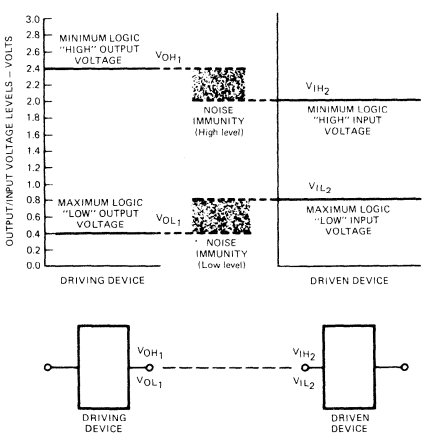
NC = No Connection

MSI INTERFACING RULES

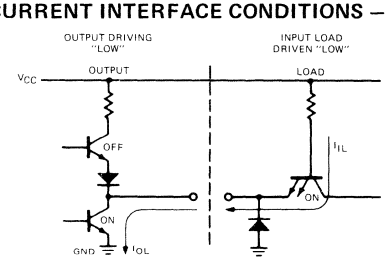
INTERFACING DIGITAL FAMILY	EQUIVALENT INPUT UNIT LOAD HIGH	EQUIVALENT INPUT UNIT LOAD LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

INPUT/OUTPUT INTERFACE CONDITIONS

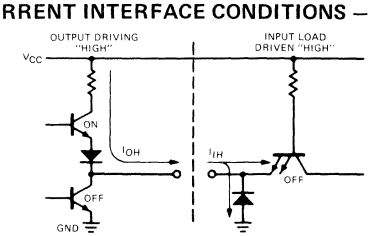
VOLTAGE INTERFACE CONDITIONS – LOW & HIGH



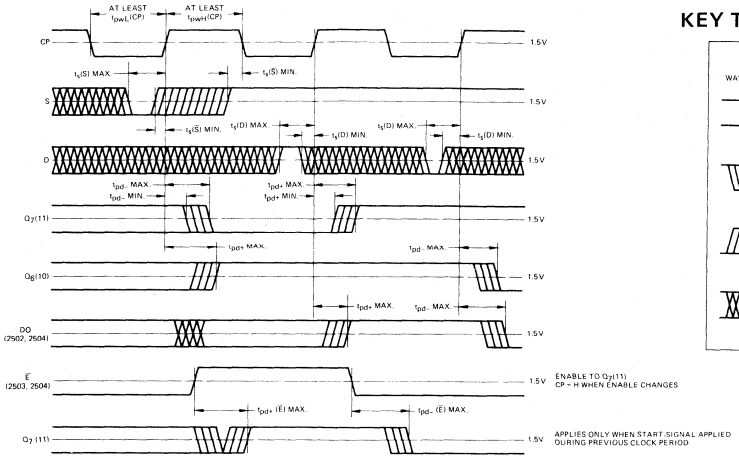
CURRENT INTERFACE CONDITIONS – LOW



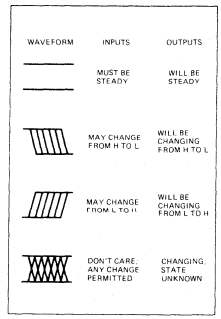
CURRENT INTERFACE CONDITIONS – HIGH



SWITCHING TIME WAVEFORMS



KEY TO TIMING DIAGRAM



DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

CP The clock input of the register.

$\overline{CC}$ The conversion complete output. This output remains HIGH during a conversion and goes LOW when a conversion is complete.

D The serial data input of the regiter.

$\overline{E}$ The register enable. This input is used to expand the length of the register and when HIGH forces the $Q_7(11)$ register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (Ground).

$Q_7(11)$ The true output of the MSB of the register.

$\overline{Q}_7(11)$ The complement output of the MSB of the register.

Q_i i = 7(11) to 0 The outputs of the register.

$\overline{S}$ The start input. If the start input is held LOW for at least a clock period the register will be reset to $Q_7(11)$ LOW and all the remaining outputs HIGH. A start pulse that is LOW for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

DO The serial data output. (The D input delayed one bit).

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS: (Measured at the 1.5V logic level).

t_{pd-} The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition.

t_{pd+} The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition.

$t_{pd-}(\overline{E})$ The propagation delay from the Enable signal HIGH-LOW transition to the $Q_7(11)$ output signal HIGH-LOW transition.

$t_{pd+}(\overline{E})$ The propagation delay from the Enable signal LOW-HIGH transition to $Q_7(11)$ output signal LOW-HIGH transition.

$t_s(D)$ Set-up time required for the logic level to be present at the data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between t_s max, and t_s min. before the clock.

$t_s(\overline{S})$ Set-up time required for a LOW level to be present at the $\overline{S}$ input prior to the clock transition from LOW to HIGH in order for the register to be reset, or time required for a HIGH level to be present on S before the HIGH to LOW clock transition to prevent resetting.

$t_{pw}CP)$ The minimum clock pulse width (LOW or HIGH) required for proper register operation.

2502/3 TRUTH TABLE

TIME	INPUTS			OUTPUTS									
t_n	D	$\overline{S}$	$\overline{E}$	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

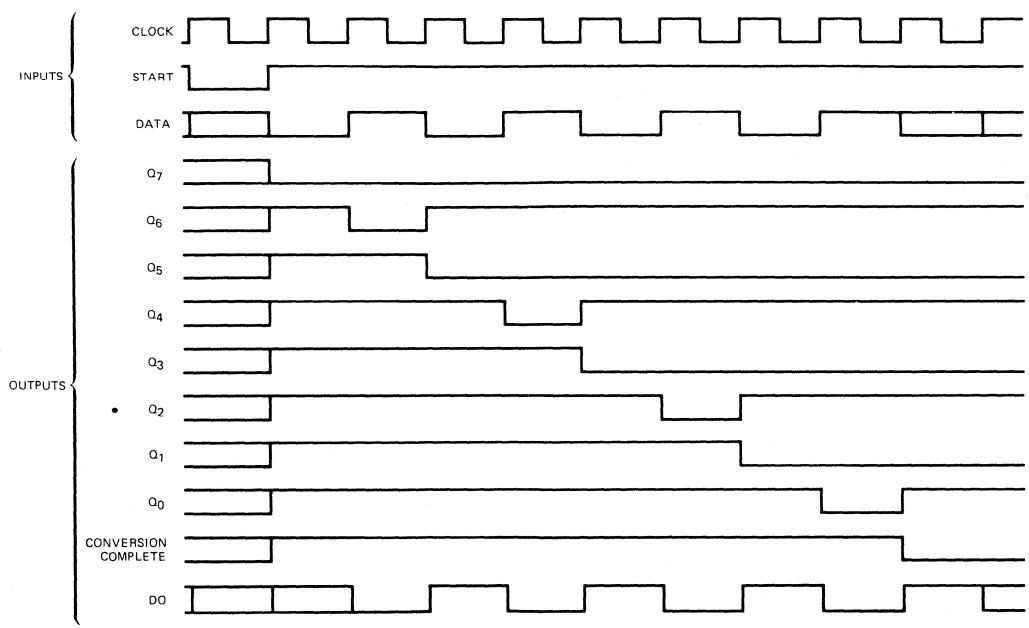
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change

Note: Truth Table for 2504 is extended to include 12 outputs.

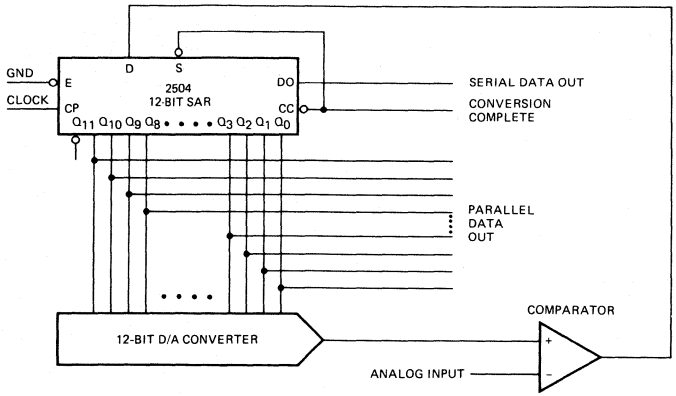
USER NOTES FOR A/D CONVERSION

1. The register can be used with either current switches that require a low voltage level to turn the switch on, or current switches that require a high voltage level to turn the current switch on. If current switches are used which turn on with a low logic level the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a high logic level then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of ±½LSB the comparator must be biased. If current switches that require a high voltage level to turn on are used, the comparator should be biased +½LSB and if the current switches require a high logic level to turn on then the comparator must be biased -½LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion.
4. The register can be used to perform 2's complement conversion by offsetting the comparator ½ full range +½LSB and using the complement of the MSB Q_7(11) as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of $\overline{CC}$ and the appropriate register output.

2502/3 TIMING CHART



2502/3/4 APPLICATION
CONTINUOUS CONVERSION ANALOG-TO-DIGITAL CONVERTER

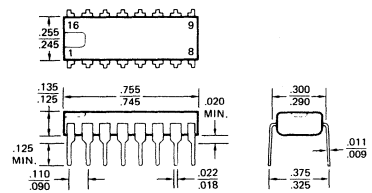


This shows how the 2502/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed continuous conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator with typical conversion rates of 100,000 conversions per second. A 10-bit continuous conversion can be performed by connecting Q_1 to Q_3 and using Q_1 as the conversion complete signal.

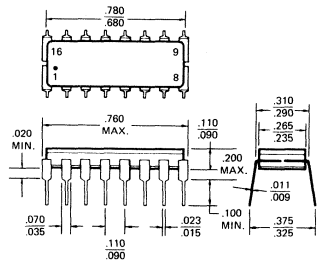
PHYSICAL DIMENSIONS

2502/3

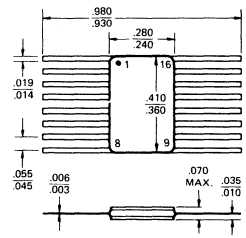
16-PIN MOLDED DIP



16-PIN HERMETIC DIP

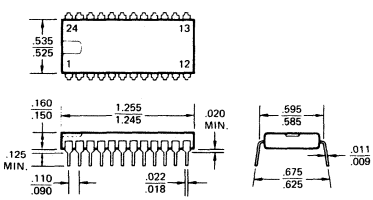


16-PIN FLAT PAK

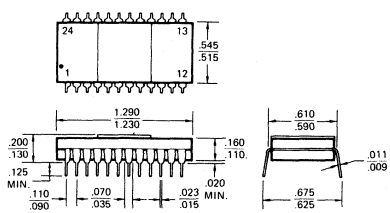


2504

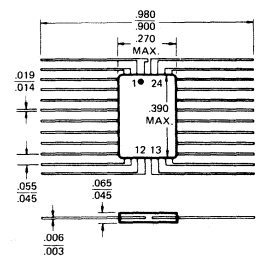
24-PIN MOLDED DIP



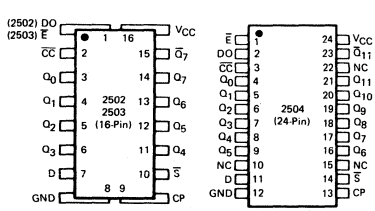
24-PIN HERMETIC DIP



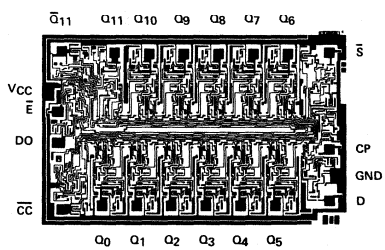
24-PIN FLAT PAK



CONNECTION DIAGRAMS
Top View



METALLIZATION AND PAD LAYOUT



Die size 0.95" x 0.142"

HIGH IMPEDANCE OPERATIONAL AMPLIFIERS

Intersil **2600 2620**
2602 2622
2605 2625

FEATURES

- Input Impedance – 500MΩ
- Offset Current – 1nA
- Bias Current – 1nA
- Gain Bandwidth Product – 100MHz
- High Gain – 150K
- Output Short Circuit Protection
- Meets MIL-STD-883

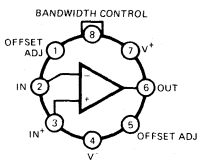
GENERAL DESCRIPTION

The 2600 series of high impedance operational amplifiers are monolithic integrated circuits fabricated using dielectric isolation. These internally compensated amplifiers feature excellent input parameters, low input bias and wide bandwidth. They are ideally suited for general purpose use in instrumentation and signal processing applications.

2600 through 2605 are compensated for unity gain. 2620 through 2625 are intended for closed loop gains of 5 or greater and feature increased slew rated and gain-bandwidth products.

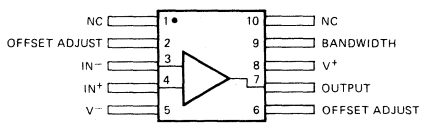
CONNECTION DIAGRAMS, TOP VIEWS

TO-99

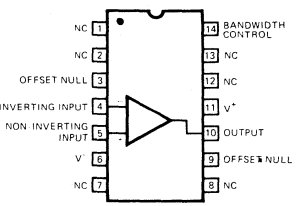


Case Connected to V^-

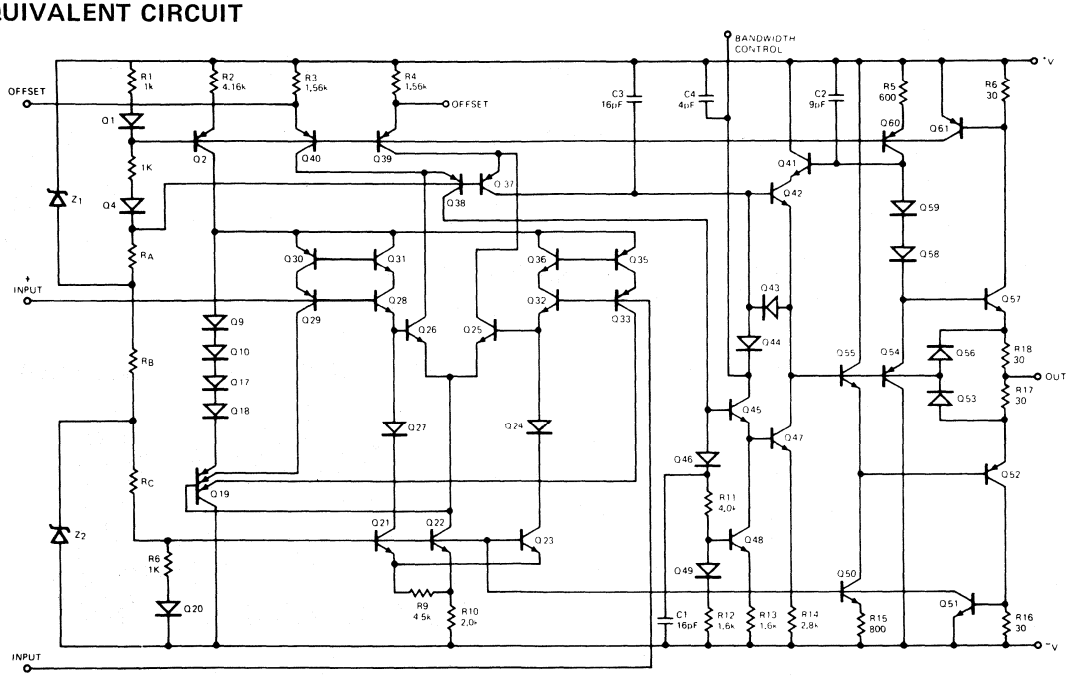
TO-91 Flat Pack



14 Pin CerDIP



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

2600
2602
2605

Supply Voltage	±22.5V
Input Voltage (Note 1)	±15V
Differential Input Voltage	±12V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	300mW
Lead Temperature (Soldering, 60 sec.)	+300°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	-55°C to +125°C (2600, 2602) 0°C to +75°C (2605)

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±15V, unless otherwise specified)

PARAMETER	CONDITIONS	2600			2602			2605			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10k\Omega$		0.5	4		3	5		3	5	mV
Input Offset Current			1	10		5	25		5	25	nA
Input Bias Current			1	10		5	25		5	25	nA
Input Resistance		100	500		40	300		40	300		MΩ
Large Signal Voltage Gain	R_L = 2kΩ, V_O = ±10V	100k	150k		80k	150k		80k	150k		V/V
Unity Gain Bandwidth	V_O < 90mV		12			12			12		MHz
Full Power Bandwidth	R_L = 2kΩ, C_L = 50pF, V_O = $20V_{p-p}$	50	75		50	75		50	75		kHz
Rise Time (Note 3)	R_L = 2kΩ, C_L = 100pF		30	60		30	60		30	60	nsec
Overshoot (Note 4)	R_L = 2kΩ, C_L = 100pF		25	40		25	50		25	50	%
Slew Rate	R_L = 2kΩ, C_L = 100pF, V_O = ±5V	4	7		4	7		4	7		V/μs
Setting Time	R_L = 2kΩ, C_L = 100pF, V_O = ±5V		1.5			1.5			1.5		nsec
(to ±10mV of Final Value)											
Output Current	V_O = ±10V	±15	±22		±10	±18		±10	±18		mA
Supply Current			3	3.7		3	4		3	4	mA
THE FOLLOWING SPECIFICATIONS APPLY FOR OPERATING TEMPERATURE RANGE											
Input Offset Voltage	$R_S \leq 10k\Omega$		2	6			7			7	mV
Input Offset Current			5	30			60			40	nA
Input Bias Current			10	30			60			40	nA
Offset Voltage Average Drift	$R_S \leq 10k\Omega$		5								μV/°C
Common Mode Rejection Ratio	V_{CM} = ±5V	80	100		74	100		74	100		dB
Common Mode Range		±11			±11			±11			V
Supply Voltage Rejection Ratio	V_S = ±9V To ±15V	80	90		74	90		74	90		dB
Large Signal Voltage Gain	R_L = 2kΩ, V_O = ±10V	70k			60k			70k			V/V
Output Voltage Swing	R_L = 2kΩ	±10	±12		±10	±12		±10	±12		V

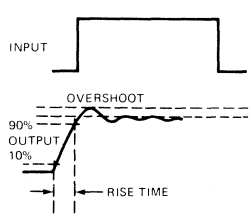
NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 2: Derate TO-91 at 4.5 mW/°C above 84°C; derate TO-99 at 6.6 mW/°C above 105°C.

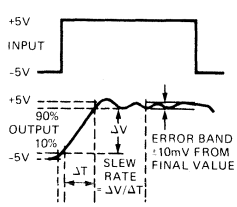
NOTE 3: V_O = 400 mV_{p-p}

NOTE 4: V_O = 800 mV_{p-p}

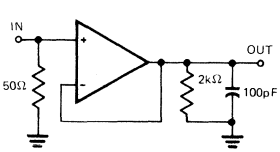
TRANSIENT RESPONSE



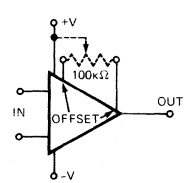
SLEW RATE AND SETTLING TIME



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

ABSOLUTE MAXIMUM RATINGS

2620
2622
2625

Supply Voltage	±22.5V
Input Voltage (Note 1)	±15V
Differential Input Voltage	±12V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	300mW
Lead Temperature (Soldering, 60 sec.)	300°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C (2620, 2622) 0°C to +75°C (2625)

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±15V, unless otherwise specified)

PARAMETER	CONDITIONS	2620			2622			2625			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 3)	$R_S \leq 10k\Omega$		0.5	4		3	5		3	5	mV
Input Offset Current			1	15		5	25		5	25	nA
Input Bias Current			1	15		5	25		5	25	nA
Input Resistance		65	500		40	300		40	300		MΩ
Large Signal Voltage Gain	R_L = 2kΩ, V_O = ±10V, C_L = 50pF	100k	150k		80k	150k		80k	150k		V/V
Gain Bandwidth (Notes 4 and 5)	R_L = 2kΩ, C_L = 50pF		100			100			100		MHz
Full Power Bandwidth	R_L = 2kΩ, C_L = 50pF, $V_O = 20V_{p-p}$	400	600		320	600		320	600		kHz
Rise Time (Note 6)	R_L = 2kΩ, C_L = 50pF		17	45		17	45		17	45	nsec
Slew Rate (Note 6)	R_L = 2kΩ, C_L = 50pF, V_O = ±5.0V	±25	±35		±20	±35		±20	±35		V/μs
Output Current	V_O = ±10V	±15	±22		±10	±18		±10	±18		mA
Supply Current			3	3.7		3	4		3	4	mA
THE FOLLOWING SPECIFICATIONS APPLY FOR OPERATING TEMPERATURE RANGE											
Input Offset Voltage	$R_S \leq 10k\Omega$			6			7			7	mV
Input Offset Current			5	35			60			40	nA
Input Bias Current			10	35			60			40	nA
Common Mode Rejection Ratio	V_{CM} = ±5V	80	100		74	100		74	100		dB
Common Mode Range		±11			±11			±11			V
Supply Voltage Rejection Ratio	V_{Supply} = ±9V To ±15V	80	90		74	90		74	90		dB
Large Signal Voltage Gain	R_L = 2kΩ, V_O = +10V, C_L = 50pF	70k			60k			70k			V/V
Output Voltage Swing	R_L = 2kΩ, C_L = 50pF	±10	±12		±10	±12		±10	±12		V

NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 2: Derate TO-91 at 4.5 mW/°C above 84°C; derate TO-99 at 6.6 mW/°C above 105°C.

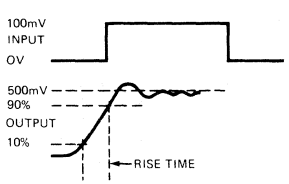
NOTE 3: May be externally adjusted to zero.

NOTE 4: V_O < 90mV.

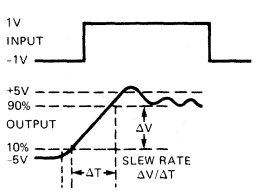
NOTE 5: 40dB gain.

NOTE 6: A_V = 5.0V.

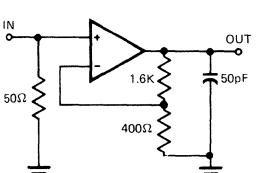
TRANSIENT RESPONSE



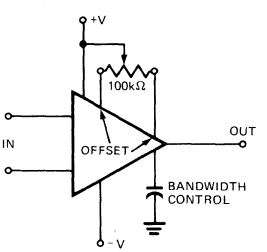
SLEW RATE



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST AND BANDWIDTH CONTROL HOOK-UP



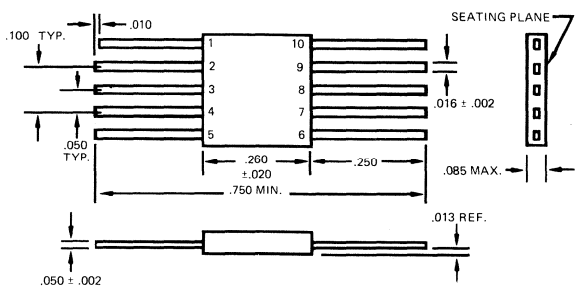
NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBER
2600	−55°C to +125°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2600-2 HA9-2600-2 HA1-2600-2
2602	−55°C to +125°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2602-2 HA9-2602-2 HA1-2602-2
2605	0°C to +75°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2605-5 HA9-2605-5 HA1-2605-5
2620	−55°C to +125°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2620-2 HA9-2620-2 HA1-2620-2
2622	−55°C to +125°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2622-2 HA9-2622-2 HA1-2622-2
2625	0°C to +75°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2625-5 HA9-2625-5 HA1-2625-5

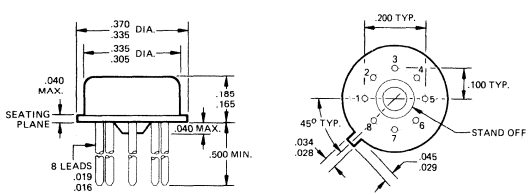
PACKAGE DIMENSIONS

TO-91 Flat Pack



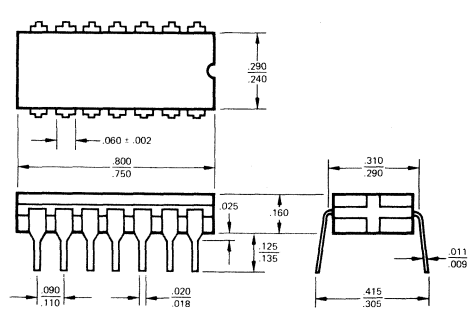
ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS ±.010 UNLESS OTHERWISE SHOWN.

TO-99 Package



NOTES: All dimensions in inches.
Leads are gold-plated Kovar.

14-Pin CerDIP



PRECISION PAIR FOR A-D CONVERTERS

3½ DIGIT PAIR 8052/8053

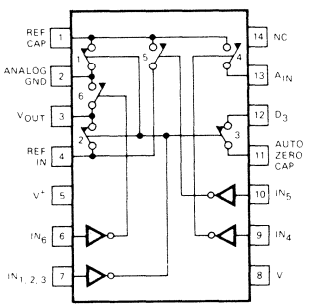
4½ DIGIT PAIR 8052A/8053A

FEATURES

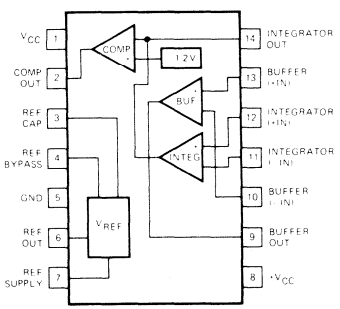
- Accuracy high enough for ±40,000 count instruments
- Priced low enough to compete with 3½ digit DPM/DVM pairs
- One basic circuit for an entire family of DVMs
- Auto-Zero; Auto-Polarity
- 5pA input current typical
- Single reference voltage
- True ratiometric (scale factor of 1)

CONNECTION DIAGRAM

8053 Auto Zero Switch Network



8052 Analog Signal Conditioner



GENERAL DESCRIPTION

The 8052/8053 pair has been designed to "lock-in" the accuracy of a DVM and at the same time give the designer the freedom of using any output format his system requires. With reasonable care, the 0.001% linearity capability of the pair can be maintained in production instruments. The system uses time-proven dual-slope integration with all of its advantages: i.e., non-critical components, high rejection of noise and a-c signals, non-critical clock frequency and true ratiometric readings. At the same time it has reduced or eliminated many of the sources of error that have limited dual-slope accuracy. With the 8052/8053 pairs, critical board layout is no longer required to give low charge injection by the switches, and elaborate ground planes are not necessary to keep clock pulse transients out of the comparator circuitry. A further feature of these devices is that the DVM/DPM manufacturer can generate an entire family of instruments using only one basic p-c board with 2 or 3 jumper points. The family could include:

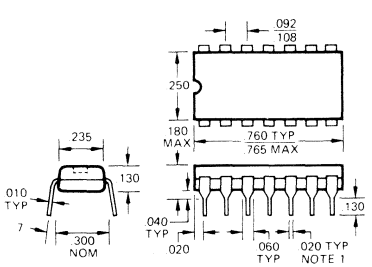
±200.0 mV Full Scale
±2.000 Volts
±400.0mV
±4.000 Volts
±800.0mV
±2.0000 Volts
±4.0000 Volts
±3.2768 Volts (16 bits in 0.1mV increments)

ORDERING INFORMATION

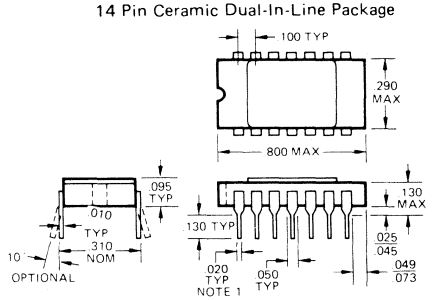
Part	Temp. Range	Package	Order Number
8052	0°C to +70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to +70°C	14 pin ceramic DIP	ICL8052CDD
8052A	0°C to +70°C	14 pin plastic DIP	ICL8052ACPD
8052A	0°C to +70°C	14 pin ceramic DIP	ICL8052ACDD
8053	0°C to +70°C	14 pin plastic DIP	ICL8053CPD
8053	0°C to +70°C	14 pin ceramic DIP	ICL8053CDD
8053A	0°C to +70°C	14 pin plastic DIP	ICL8053ACPD
8053A	0°C to +70°C	14 pin ceramic DIP	ICL8053ACDD

PACKAGE DIMENSIONS

14 Pin Plastic Dual-In-Line Package



14 Pin Ceramic Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1)	500 mW
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 60 Sec.)	300°C

8052 ONLY

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration, All Outputs (Note 3)	Indefinite

8053 ONLY

Source Current (I_S)	100 mA
Drain Current (I_D)	100 mA
Digital Inputs	5 mA
V^+ to V^-	25V
Digital Input to V^+	V^- to V^+
Digital Input to V^-	V^+ to V^-

Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

8053 ELECTRICAL CHARACTERISTICS ($V+ = +5V$, $V- = -15V$ unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8053			8053A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
R_{on} Switch 1, 2 (each Switch)	$V_7 = +4.5V$ $V_6 = V_9 = V_{10} = +0.5V$		1000	2500		1000	2500	ohms
R_{on} Switch 3	Same as Switch 1, 2		2000	5000		2000	5000	ohms
R_{on} Switch 4	$V_9 = +4.5V$ $V_6 = V_7 = V_{10} = +0.5V$		1000	2500		1000	2500	ohms
R_{on} Switch 5	$V_{10} = +4.5V$ $V_6 = V_7 = V_9 = +0.5V$		1000	2500		1000	2500	ohms
R_{on} Switch 6	$V_6 = +4.5V$ $V_7 = V_9 = V_{10} = +0.5V$		1000	2500		1000	2500	ohms
Total Leakage Sw 1, 2, 5 & 6 $I_1 + I_3$ @ most positive Voltage	$V_6 = V_7 = V_9 = V_{10} = +0.5V$ $V_4 = -4V$, $V_2 = 0V$ $V_1 = V_3 = +4V$		10	50		5	20	pA
Total Leakage Sw 1, 2, 5 & 6 $I_1 + I_3$ @ most negative Voltage	$V_6 = V_7 = V_9 = V_{10} = +0.5V$ $V_4 = +4V$, $V_2 = 0V$ $V_1 = V_3 = -4V$		10	50		5	20	pA
Total Leakage Sw 3 & 4 $I_{12}+I_{13}$ @ most positive Volt.	$V_6 = V_7 = V_9 = V_{10} = +0.5V$ $V_1 = V_{11} = -4V$ $V_{12} = V_{13} = +4V$		10	50		5	20	pA
Total Leakage Sw 3 & 4 $I_{12}+I_{13}$ @ most negative Volt.	$V_6 = V_7 = V_9 = V_{10} = +0.5V$ $V_1 = V_{11} = +4V$ $V_{12} = V_{13} = -4V$		10	50		5	20	pA
Supply Current (V^+ or V^-)	$V_{6,7,9 \text{ or } 10} = 0.5V$ (each of 4 drivers)		150	300		150	300	μA
	$V_{6,7,9 \& 10} = 4.5V$ (all drivers)		1	10		1	10	μA
Switching Time t_{on}	See Figure 1		75			75		nsec
t_{off}	See Figure 1		150			150		nsec

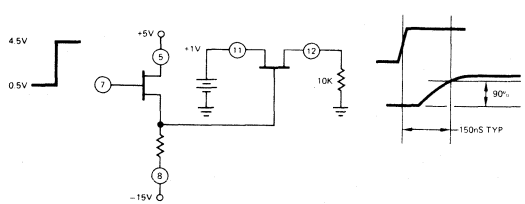
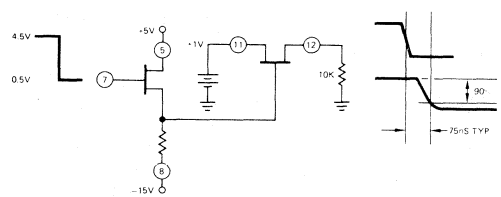


FIGURE 1. TURN-ON SWITCHING TIME.



TURN-OFF SWITCHING TIME.

8052 ELECTRICAL CHARACTERISTICS (V_s = ±15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8052			8052A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
EACH OPERATIONAL AMPLIFIER								
Input Offset Voltage	V_{CM} = 0V		20	50		20	50	mV
Input Current (either input)	V_{CM} = 0V		5	50		2	10	pA
Common-Mode Rejection Ratio	V_{CM} = ±10V		90	70		90	70	dB
Non-Linear Component of Common-Mode Rejection Ratio*	V_{CM} = ±2V		110			110		dB
Large Signal Voltage Gain	R_L = 10kΩ	20,000			20,000			V/V
Slew Rate			6			6		V/μs
Unity Gain Bandwidth			1			1		MHz
Output Short-Circuit Current			20	50		20	50	mA
COMPARATOR AMPLIFIER								
Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
Positive Output Voltage Swing		+12	+13		+12	+13		V
Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE								
Output Voltage		1.6	1.85	2.1	1.75	1.85	1.95	V
Output Resistance			5			5		ohms
Temperature Coefficient			40			20		ppm /°C
Supply Current Total			6	12		6	12	mA

*This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS

(V_{++} = +15V, V_+ = +5V, V_- = −15V Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	8052/8053(1)			8052A/8053A(2)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V	−0.000	±0.000	+0.000	−0.0000	±0.0000	+0.0000	Digital Reading
Ratiometric Reading	$V_{in} = V_{Ref.}$	+0.999	+1.000	+1.001	+0.9999	+1.0000	+1.0001	Digital Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-2V \leq V_{in} \leq +2V$		0.2	1		0.5	1	Digital Count Error
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \cong +V_{in} \approx 2V$		0.2	1		0.5	1	Digital Count Error
Noise (P-P value not exceeded 95% offtime)	V_{in} = 0V Full scale = 200.0mV		0.2					Digital Count
	Full scale = 2.000V		0.05			0.3		
Leakage Current into Input	V_{in} = 0V		5	30		3	10	pA
Zero Reading Drift	V_{in} = 0V $0° \leq T_A \leq 70°C$		1	5		0.5	2	μV/°C
Scale Factor Temperature Coefficient	V_{in} = +2V $0 \leq T_A \leq 70°C$ (ext. ref. 0 ppm/°C		3	15		2	5	ppm/°C

(1) Tested in 3½ digit (2,000 count) circuit shown in Fig. 5 clock frequency 12 kHz.

(2) Tested in 4½ digit (20,000 count) circuit shown in Fig. 5 clock frequency 120 kHz.

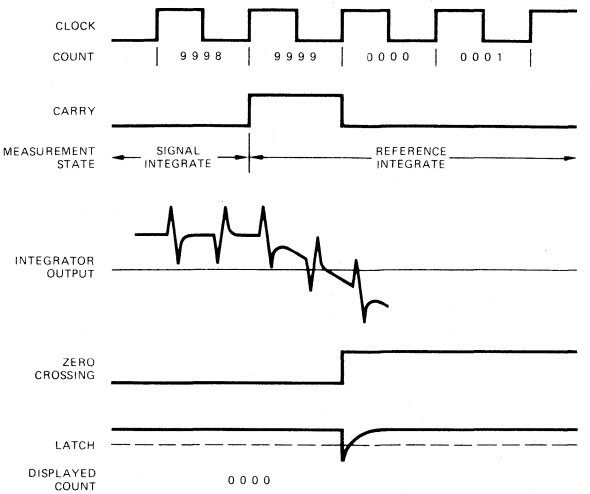


FIGURE 3.

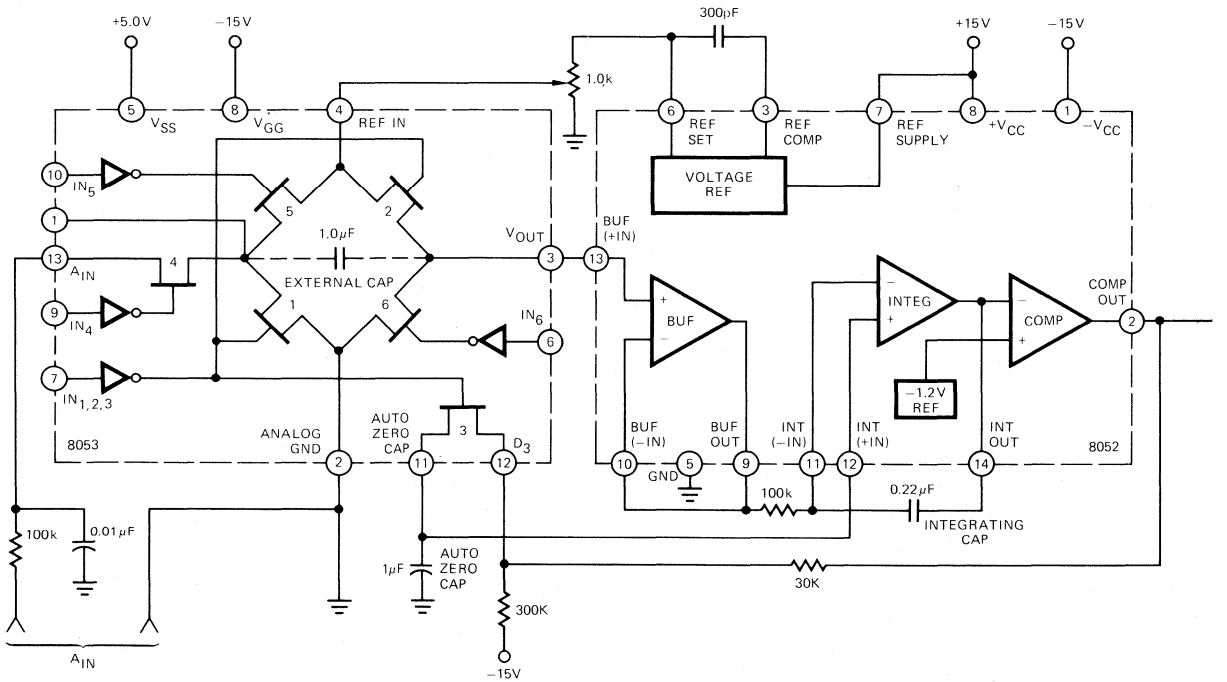
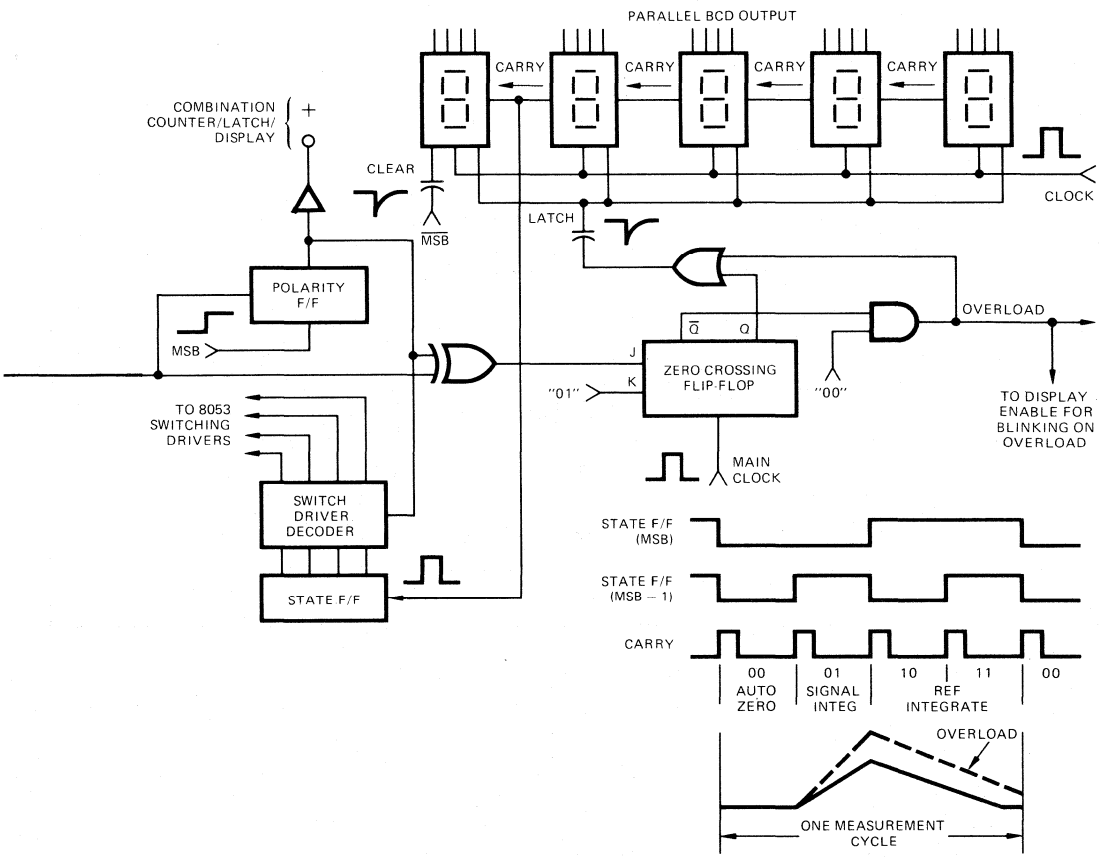


FIGURE 4. FUNCTIONAL DIAGRAM FOR A/D CONVERTER.


PARALLEL BCD OUTPUT
CARRY
CARRY
CARRY
CARRY
COMBINATION COUNTER/LATCH/ DISPLAY
+
CLEAR
MSB
CLOCK
LATCH
POLARITY F/F
MSB
OVERLOAD
Q̄
Q
J
K
ZERO CROSSING FLIP-FLOP
"01"
"00"
TO DISPLAY ENABLE FOR BLINKING ON OVERLOAD
TO 8053 SWITCHING DRIVERS
MAIN CLOCK
SWITCH DRIVER DECODER
STATE F/F
STATE F/F (MSB)
STATE F/F (MSB – 1)
CARRY
00 AUTO ZERO
01 SIGNAL INTEG
10
11
REF INTEGRATE
00
OVERLOAD
ONE MEASUREMENT CYCLE

THEORY OF OPERATION

Figure 4 shows a function diagram for an A-D converter using the 8052/8053 pair. In this circuit, each measurement cycle is divided into four equal parts by the state F/F. The first part, state 00, is the auto-zero cycle. The switch driver decoder recognizes this state and turns on hex switches number 1, 2, and 3. Switches 1 and 2 impress a voltage equal to V_{REF} across the reference capacitor. Switch 3 closes a loop around the integrator and comparator. The purpose of this loop is to charge up the auto-zero capacitor until the integrator output does not change with time. During the second state, 01, switches 1, 2 and 3 are opened and switch 4 is closed. If the input voltage is zero, the buffer, integrator and comparator will see the same voltages that existed in the previous state. Thus, the integrator output will not change but will remain stationary during the entire signal-integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the auto-zero cycle and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this cycle, the sign of the ramp is latched into the polarity F/F. The final cycle, reference integrate, includes states 10 and 11. The switch driver decoder uses the output of the polarity F/F in deciding whether to close switch 5 or 6. If the input signal was positive, switch 6 is closed and a voltage which is V_{REF} more negative than during auto-zero is impressed on the buffer input. If the input signal was negative switch 5 is closed and a voltage which is V_{REF} more positive than during auto-zero is impressed on the buffer input. Thus, the reference capacitor generates the equivalent of a (+) reference or a (–) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to zero. The time, or number of counts, required to do this is proportional to the input voltage. Since the reference cycle can be twice as long as the signal integrate cycle, the input voltage required to give a full scale reading $\equiv 2\ V_{REF}$. The circuit, as described to this point, is not new to this application. It has been used successfully for several years. However, this system makes three major contributions to the accuracy of this circuit. These are: (1) low charge injection, (2) junction FET op amp, and (3) zero-crossing flip-flop.

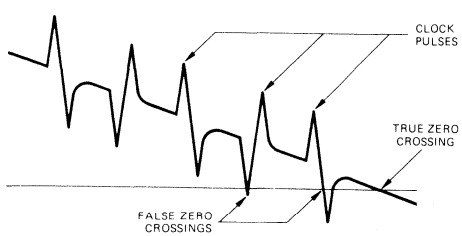


FIGURE 2.
INTEGRATOR OUTPUT NEAR ZERO-CROSSING.

1. Low Charge Injection.

During auto-zero, there is no problem in charging the capacitors to the correct voltage. The problem is getting the switches off without changing this voltage. As the gate is driven off, the gate-to-drain capacitance of the switch injects a charge on the reference or auto-zero capacitor, changing its voltage. The designer, using discrete components, is forced into critical board layouts where charges of opposite polarity are injected to compensate or neutralize the driver injection. This balance will be upset by any unit-to-unit variation of switch capacitance so at best the final design is a compromise. In the 8052/8053 the critical layout has been done on the semiconductor chip and need not concern the user. Also, since a silicon-gate process is used for the switches, the unit-to-unit variation is extremely low. The net result is to give an error due to charge injection that is so low it is difficult to measure; but certainly less than 5μV referred to the input.

2. Junction FET Op Amps.

Both the buffer and integrator use junction FET inputs in a guarded circuit that reduces the voltage across the FET to 3 or 4 volts. At this voltage level, input leakage currents of 2 pA are typical. For typical component values 2 pA leakege contributes less than 2 μV of error to the circuit. In theory, MOS FET's would contribute less leakage but their increased noise would swamp out any improvement by orders of magnitude.

3. Zero-Crossing Flip Flop.

The problem that the zero-crossing flip-flop is designed to solve is shown in figure 2.

The integrator output is approaching the zero-crossing point where the clock will be stopped and the reading displayed. The clock pulse feedthrough superimposed upon this ramp will cause a false reading by stopping the count prematurely. For a 40,000 count instrument, the ramp is changing approximately 0.25mV per clock pulse (10 volt max integrator output divided by 40,000 counts). The clock pulses have to be less than 100μV peak to avoid causing significant errors. The circuit layout to achieve this can be time consuming at best and impossible at worst. The suggested circuit gets around this problem by feeding the zero-crossing information into a J-K flip-flop instead of using it directly. The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. Any false zero-crossing caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by one count in every instance. If a correction was not made, the display would always be one count too high. The correction is to change the four states of the converter one count early. In other words, instead of changing states at the beginning of count 0000, the states are changed at the beginning of count 9999. Since this pulse is always available as "carry" from a synchronous counter, no extra decoding is required. A bonus feature of this circuit is that latching the counter output becomes very simple with no potential race condition existing. The designer has one complete clock pulse to transfer the counter data to the latches and decouple them before a false reading will occur. The timing diagram for a signal ≈ 0 is shown in figure 3.

APPLICATIONS

Specific Circuits Using the 8052/8053

Figure 5 shows the complete circuit for a 4-1/2 digit (±2.000V full scale) A-D with LED readout and parallel BCD data lines. In addition to the 8052/8053, this circuit uses 6 low-cost CMOS packages for control and 5 TIL 306 as a combination LED readout, synchronous counter, and BCD latch. In this circuit, the clock runs continuously driving the 5 decade counters in the TIL 306's. The carry from the fourth decade is used to trigger the state F-F. Thus, each of the four states lasts for 10,000 counts. At the beginning of state 10, the 5th decade is cleared. None of the other counters need to be cleared since they automatically roll to 0000 at this point. When the zero-crossing F-F detects the end of the measurement, a latch pulse is initiated. The R-C time constant of this pulse is selected long enough (50nSec) to assure the latches turn on, but short enough (3μSec) to assure that the latches are decoupled before the next clock pulse. Selecting a typical time constant of 400nSec assures proper latching with wide variance in component value.

In order to give a visual indication of overload, the LED displays are blanked during state 00 if an overload exists. If overloaded, the instrument will blink a reading of 19999. A non-blinking reading of 19999 is a valid reading for the instrument.

By tying the clear terminals of the state flip-flop and the four decade counters to a common bus, the instrument can be synchronized to external events. If the bus is low, the instrument is held in auto-zero with the last measurement cycle at the beginning of state 00. The data valid pulse indicates the end of measurement cycle. For free-running condition, the bus is held high at +5 volts.

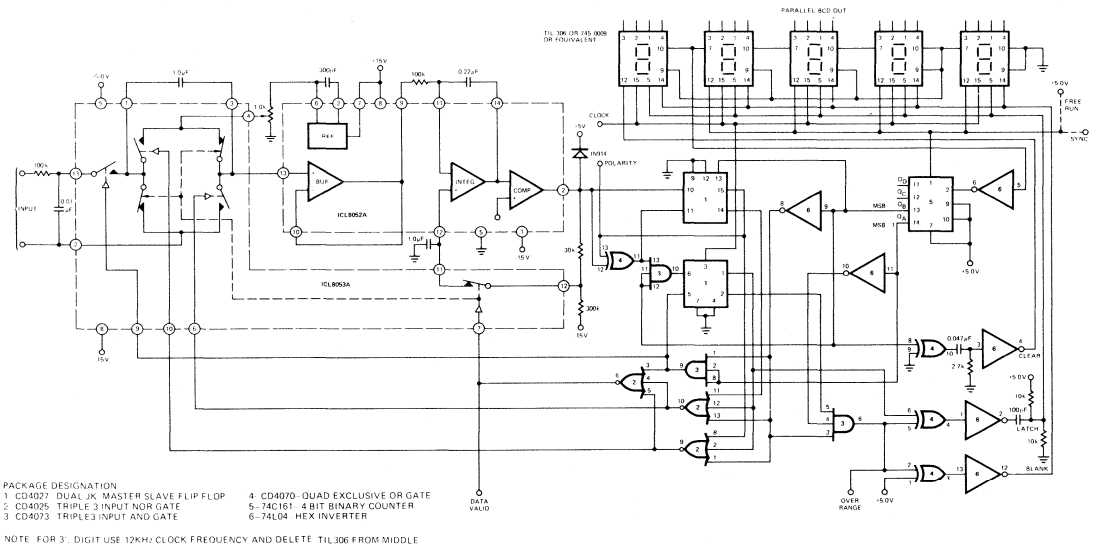


FIGURE 5. GENERAL CIRCUIT FOR A FAMILY OF DVM's.

Generating a Family of A-D Converters

In figure 5, the lines marked (MSB) and (MSB-1) are connected to Q_B and Q_A of the 4-bit state flip-flop respectively. This forces a change in state for each carry pulse (10,000 counts) from the decade counters. If the lines were moved to Q_C and Q_B respectively, two carry pulses (20,000 counts) would be required to change states. Since full-scale is two states long, the max count now becomes 40,000; (actually 39,999). Similarly if Q_D and Q_C are used the max count is now 7,999 (one less decade counter would be used in this case). The ability to easily change max count (full scale) is most useful where the A-D converter is measuring physical constants such as temperature, distances, weight, etc. It allows designer to match the digital reading of the instrument to the analog range of the transducer. Since the analog input required to generate full scale output is $2V_{REF}$ in every case, an almost endless variety of scale factors can be generated easily from one basic design. Table I summarizes how the family of DVM's is generated.

Full Scale	V_{REF}	Total Number Of Decade Counters	Connect MSB-1 to	Connect MSB to
±200.0mV	+.1000V	4	Q_A	Q_B
±2.000V	+1.000V	4	Q_A	Q_B
±400.0mV	+.2000V	4	Q_B	Q_C
±4.000V	−2.000V	4	Q_B	Q_C
±800.0mV	+.4000V	4	Q_C	Q_D
±2.0000V	+1.0000V	5	Q_A	Q_B
±4.0000V	−2.0000V	5	Q_B	Q_C
±3.2768V	+1.6384V	4*	Q_C	Q_D

*Number of 4-bit binary counters

TABLE I

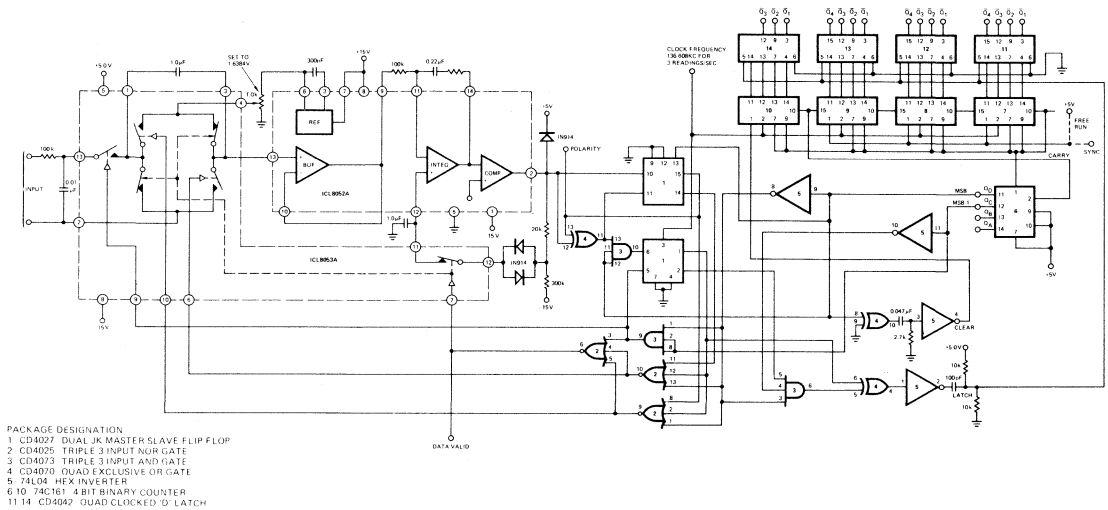


FIGURE 6. 16-BIT BINARY CONVERTER

Specific circuits demonstrating this principle are shown in figures 5 and 6. An 800.0mV full scale A-D can be obtained from the 2.0000V instrument shown in figure 5 with the three following modifications:

1. Delete middle LED counter.
2. State decode moved to Q_D and Q_C,
3. Reference voltage adjusted to 0.4000V.

Figure 6 is the specific circuit for a 16-bit binary A-D. Here the decade counters and displays have been replaced by synchronous 4-bit counters and latches. To give a full scale reading of ±3.2768 volts the reference is adjusted to 1.6384 volts.

Figure 7 shows the circuit for a 40,000 count instrument. This circuit conforms to all of the "family" rules with the exception that it uses a −2.0000 volt reference. If a positive reference was used, pin 3 of the 8053 would have to swing to +6V (+4 volt input +2 volt reference). Since this exceeds the +5 volt supply, the switch would forward bias into the substrate. It can easily accommodate the +2 to −6 volt swing required of a negative reference. The only change required by a negative reference is that the drive to pin 6 (+ Reference driver) and pin 10 (− Reference driver) be interchanged. Also since the internal reference is not used, no connections are made to pins 3, 6, and 7 of the 8052.

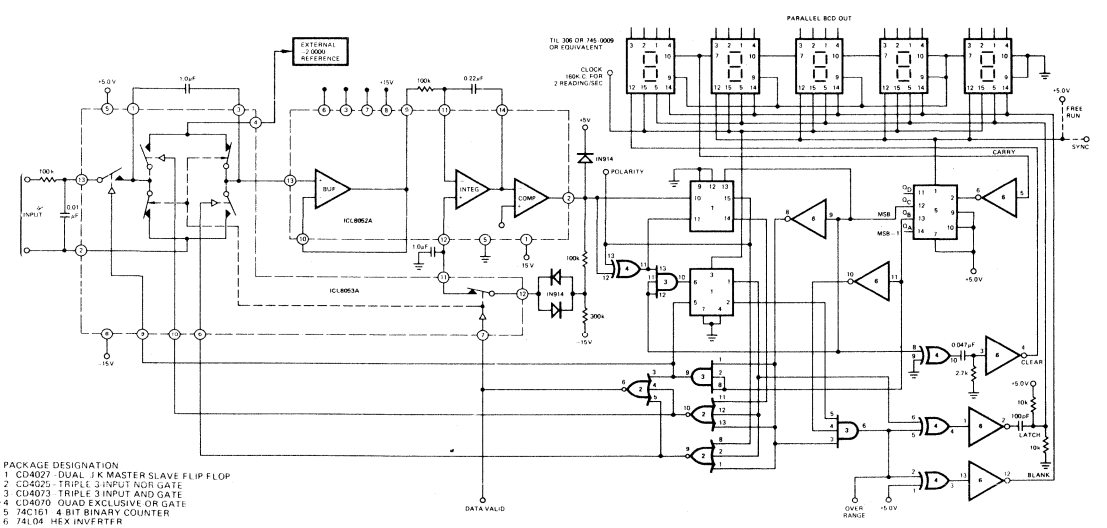


FIGURE 7. 4¾ DIGIT DVM

Alternate Circuits

In a 4½ digit (20,000 count) instrument where the family generating capabilities of the four bit counter is not required, a dual D flip-flop can be substituted for this function with some reduction in parts costs. Also a "±1" LED, driven by a dual D flip-flop, can replace the fifth TIL306. Figure 8 shows a circuit with these two substitutions made.

If the Parallel BCD capabilities of the TIL306 are not required, a further reduction in parts cost can be achieved by using the circuit of figure 9. In this circuit the MM74C926 performs the counting, latch and 7 segment decode function of the TIL306 such that it can be used with any LED displays. Some modification of the clock and latch circuit is required since the 74C926 uses a ripple counter with a carry at 0000 instead of a synchronous carry at 9999. When a zero-crossing signal is detected and the latch-enable is initiated, a signal is simultaneously fed to the clock drive circuitry to delay the clock and therefore the count until the previous count can be latched. The latch time-constant is shorter than the clock-delay time-constant to assure that the latch is transferred and disabled before the clock resumes counting. A 1μS time delay in the output of the clock driver assures that the slight delay (100nS) between the clock pulse and the clock-delay pulse does not clock the counter. Blanking is provided to give a visual indication of overload. However, the display will flash .0000 instead of 1.9999 due to the nature of the ripple counter.

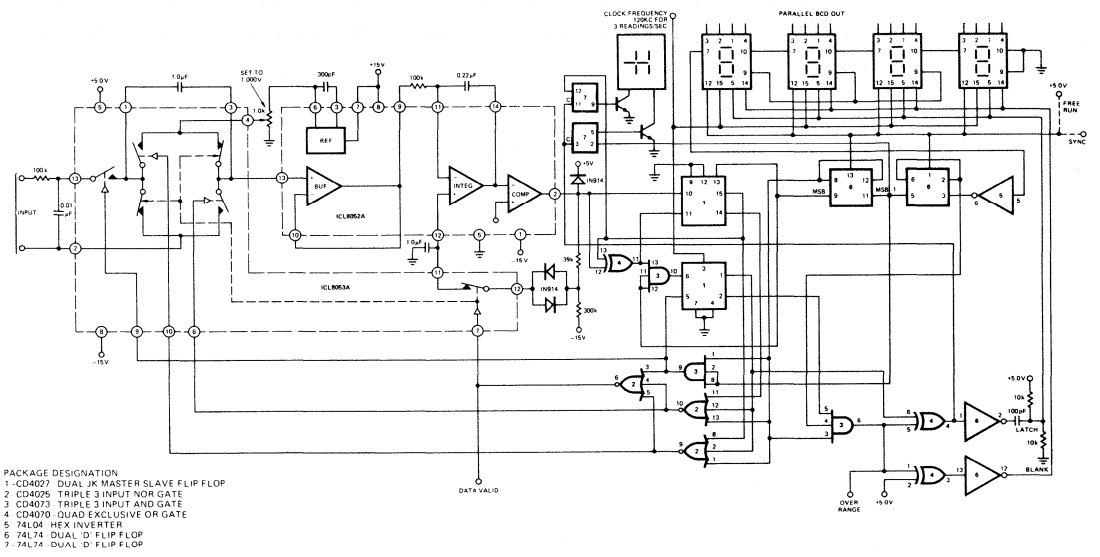


FIGURE 8. 4½ DIGIT DVM (PARALLEL BCD)

Component Selection

Except for the Reference Voltage, none of the component values are first-order important in determining the accuracy of the instrument. While this is undoubtedly an advantage of this approach, it does make the selection of nominal component values arbitrary at best. For instance the reference capacitor and auto-zero capacitor are each shown as 1.0μF. These relative large values are selected to give greater immunity to PC board leakage since much smaller capacitors are adequate for charge injection errors or leakage errors from the 8052/8053. The ratio of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at ±14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. Again the .22 value for integrating cap is selected for PC considerations alone since the very small leakage at the integrator input is nulled at auto-zero. A very important characteristic of the integrating cap is low dielectric absorption. A polypropylene cap (made by TRW) gave excellent results in the application. In fact a good test for dielectric absorption is to test the subject cap in this circuit with the input tied to reference. This ratiometric condition should read 1.0000 and any deviation is probably due to dielectric absorption. In this test poly-carbonate caps typically read .9992, polystyrene, .9997 and polypropylene, 1.0000. The increased temperature coefficient of polypropylene is of no consequence in this circuit. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

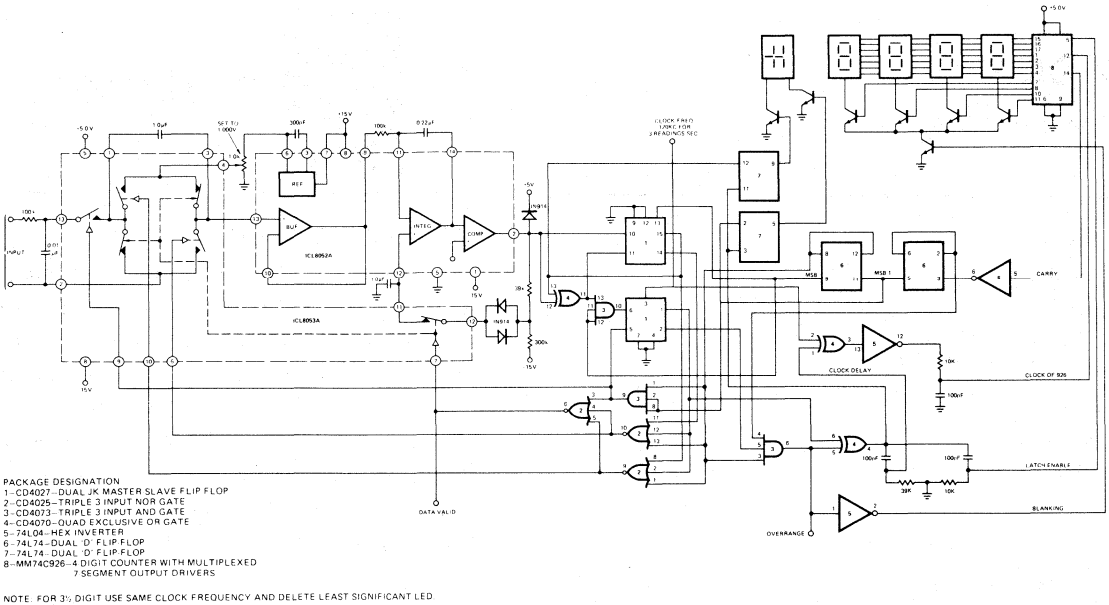


FIGURE 9. 4½ DIGIT DVM (20,000 COUNT MULTIPLEXED DISPLAY)

The output of the comparator is clamped to the +5 volts supply to prevent the positive swing of the comparator from forward biasing the auto-zero switch to its substrate and injecting minority carriers that would be collected as leakage currents. In addition, a voltage translation network connects the output of the comparator to the auto-zero switch. The purpose of this network is to assure that, during auto-zero, the output of the comparator is at or near the threshold of the CMOS logic (+2.5V) while the auto-zero cap is being charged to V_{REF} (+1V in the case of 2.0000 instrument). Otherwise even with zero signal in, some reference integrate period would be required to drive the comparator output to the threshold region. This would show up as an equivalent offset error. Once the divider chain has been selected, the unit-to-unit variation should contribute less than a few tenths-of-a-count error in the worse case (40,000 count instrument) and proportionately less in other instruments. For a 3½ digit instrument, the error is unmeasurable.

Finally, the back-to-back diodes are used to lower noise. In the normal operating mode they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero cap. At start-up or recovery from an overload, their impedance is low to large signals so the cap can be charged in one auto-zero cycle.

Max Clock Frequency

The maximum conversion rate of most dual-slope A-D converters is limited by the frequency response of the comparator. Even though the comparator in this circuit is all NPN with an open-loop gain-bandwidth product of 300MHz, it is no exception. The comparator output follows the integrator ramp with a 3μS delay. At a clock frequency of 160kHz (6μS period) half of the first reference integrate period is lost in delay. This means that the meter reading will change from 0 to 1 with 50μV in, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at midpoint is considered desirable by most users. However, if the clock frequency is increased appreciably above this, the instrument will flash "1" on noise peaks even when the input is shorted.

Some circuits use positive feedback or a latch to solve the delay problem. However, unless the comparator voltage swing, the comparator gain, and the integrator gain are carefully controlled, this circuit can generate *anticipation* errors that greatly exceed the 3μS *delay* error. Also it is very susceptible to noise spikes. A more controlled approach for extending the conversion rate is the use of a small resistor in the integrator feedback loop. This feeds a small pulse to the comparator to get it moving quickly, and partially compensate for its delay.

The minimum clock frequency is established by leakage on the auto-zero and reference cap. With most devices, measurement cycles as long as 10 seconds gave no measurable leakage error.

3½ DIGIT A/D PAIR

8052/7101

FEATURES

- Guaranteed zero reading for 0 volts input
- Auto-zero; auto polarity
- 5pA input current typical
- Single reference voltage
- Latched parallel (full-time) BCD output for LCDs or data busing
- True polarity at zero count for precise null detection
- On-board clock and reference

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to 70°C	14 pin ceramic DIP	ICL8052CDD
7101	0°C to 70°C	40 pin plastic DIP	ICL7101CPL
7101	0°C to 70°C	40 pin ceramic DIP	ICL7101CDL

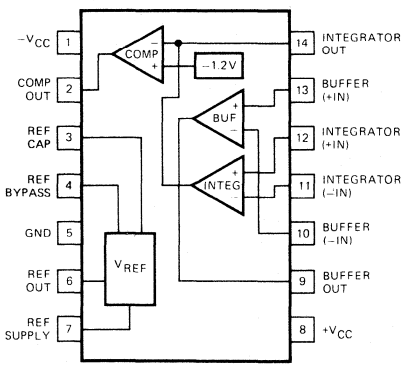
GENERAL DESCRIPTION

The 8052/7101 A/D Pair, with its parallel BCD outputs, is ideally suited for data processing applications or interfacing with 3½-digit Liquid Crystal Displays. No external circuitry is required to demultiplex the information. In addition, it has a "start/reset" input and "busy" output that allows easy synchronization to system requirements. The 8052/7101 provides 4½-digit accuracy in a 3½-digit format with typical system performance like 5pA input leakage, auto-zero to 10μV with less than 1μV/°C drift and Linearity to 0.002%.

The 8052/7101 A/D pair also features conversion rates from 10 seconds to 30 per second, making them ideally suited for a wide variety of applications.

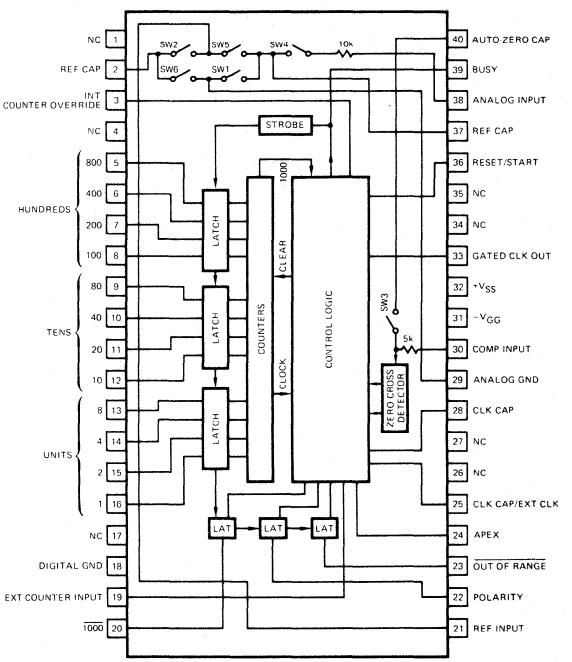
CONNECTION DIAGRAM

8052 Analog Signal Conditioner



CONNECTION DIAGRAM

7101 Digital Processor



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1)	500mW
Storage Temperature	−65°C to +150°C
8052 ONLY	
Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration, All Outputs (Note 3)	Indefinite
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 60 Sec.)	300°C
7101 ONLY	
Source Current (I_S)	100mA
Drain Current (I_D)	100mA
Digital Inputs	5mA
V^+ to V^-	25V
Digital Input	V^- to V^+

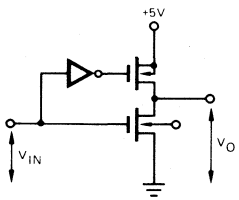
Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

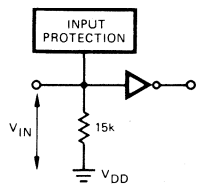
Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

7101 ELECTRICAL CHARACTERISTICS ($V^+ = +5.0V$, $V^- = -15V$, $T_A = +25°C$ unless otherwise specified)

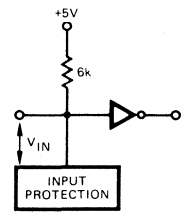
PARAMETER	SYMBOL	CONDITIONS	7101			UNITS
			MIN	TYP	MAX	
Clock Frequency	f_{IN}	C = 1500 pF		20		kHz
External Clock In	I_{INL}	V_{IN} = 0 V		0.35	1.0	mA
External Clock In	I_{INH}	V_{IN} = +5.0 V		0.35	1.0	mA
Reset/Start	I_{INL}	V_{IN} = 0 V		0.8	2.0	mA
Internal Counter Override External Counter Input	I_{INH}	V_{IN} = +5.0 V		0.35	1.0	mA
BCD	V_{OL}	I_{OL} = 1.6 mA		0.25	0.4	V
BCD	V_{OH}	I_{OH} = −200 μA	2.4	4.5		V
Out-of-Range	V_{OL}	I_{OL} = 3.2 mA		0.25	0.4	V
Out-of-Range	V_{OH}	I_{OH} = 400 μA	2.4	4.5		V
Polarity, Apex, Busy, $\overline{1000}$	V_{OL}	I_{OL} = 0.8 mA		0.25	0.4	
Polarity, Apex, Busy, $\overline{1000}$	V_{OH}	I_{OH} = −200 μA	2.4	4.5		V
Gated Clockout	V_{OL}	I_{OL} = 0.3 mA		0.25	0.4	V
Gated Clockout	V_{OH}	I_{OH} = −200 μA	2.4	4.5		V
Switches 1, 3, 4, 5, 6	$R_{DS(ON)}$			400		Ω
Switch 2	$R_{DS(ON)}$			2500		Ω
+5.0 V Supply Current	I_{CC}^+			15	25	mA
−15 V Supply Current	I_{CC}^-			3.0	5.0	mA



Output



External Counter Input
Internal Counter Override



Start/Reset

TYPICAL INPUT/OUTPUT SCHEMATICS

8052 ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = +25°C unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8052			UNITS
		MIN	TYP	MAX	
OPERATIONAL AMPLIFIER					
Input Offset Voltage	V_{CM} = 0V		20	50	mV
Input Current (either input)	V_{CM} = 0V		5	50	pA
Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio*	V_{CM} = ±2V		110		dB
Large Signal Voltage Gain	R_L = 10kΩ V_{OUT} = ±10V	20,000			V/V
Slew Rate			6		V/μs
Unity Gain Bandwidth			1		MHz
Output Short-Circuit Current			20	50	mA
COMPARATOR AMPLIFIER					
Small-Signal Voltage Gain	R_L = 30kΩ		4000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		-2.0	-2.6		V
VOLTAGE REFERENCE					
Output Voltage		1.5	1.75	2.0	V
Output Resistance			5		ohms
Temperature Coefficient			40		ppm
Supply Current Total			6	12	mA

*This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS

(V_{++} = +15V, V_+ = +5.0V, V_- = −15V, T_A = +25°C, Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	8052/7101 (1)			UNITS
		MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V	-0.000	±0.000	+0.000	Digital Reading
Ratiometric Reading	$V_{in} \equiv V_{Ref.}$	+0.998	+1.000	+1.001	Digital Reading
Linearity over ± Full Scale (error off reading from best straight line)	$-2V \leq V_{in} \leq +2V$		0.1	1	Digital Count Error
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 2V$		0.1	1	Digital Count Error
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 200.0mV		0.2		Digital
	Full scale = 2.000V		0.05		Count
Leakage Current into Input	V_{in} = 0V		5	30	pA
Zero Reading Drift	V_{in} = 0V $0° \leq T_A \leq 70°C$		1	5	μV/°C
Scale Factor Temperature Coefficient	V_{in} = +2V $0° \leq T_A \leq 70°C$ (ext. ref. 0 ppm/°C)		3	15	ppm/°C

(1) Tested in 3½ digit (2,000 count) circuit shown in Fig. 1 clock frequency 20kHz.

CIRCUIT DESCRIPTION

Figure 1 shows a typical circuit for a DVM. A minimum of external components is required since the chips have an on-board clock and a medium-quality (40ppm/°C) internal reference. The circuit also shows the switching required for two scale factors: 2.000V and 200.0mV full scale.

The system uses the time-proven dual-slope integration with all of its advantages, i.e., non-critical components, high rejection of noise and AC signals, non-critical clock frequency and true ratiometric readings. At the same time, it eliminates one of the basic disadvantages of dual-slope conversion: separate positive and negative reference sources. In this system, the negative reference is generated by charging the reference capacitor to the positive reference potential and then switching it into the circuit inverted when a negative reference is required. Due to the very low leakage and charge injection of the FET switches, the positive and negative references track each other to 10μV over a wide temperature range. This assures a very small error between positive and negative scale factor and, thus, excellent linearity from (+) full-scale to (–) full-scale (.002% typical).

The measurement cycle for the 8052/7101 has three phases. These are auto-zero, integrate input, and integrate reference. At the end of a measurement the system automatically reverts to the auto-zero mode until a new measurement is initiated. If an over-load has not occurred in the previous measurement, 10 milliseconds of auto-zero is sufficient to null any offsets to 10μV. At power on, or after an overload, 100 milliseconds is required to assure the auto-zero capacitor has charged to the correct value.

Start Conversion

Prior to conversion, the reset-start input must be held low to inhibit conversion (during auto-zero). Conversion is initiated by a positive transition on the start-reset line. (It must therefore return to the low state prior to completion of conversion in order to allow proper auto-zero function.) The positive transition generates a clear pulse which resets all internal logic (counters, etc.) and sets the clock enable, thus initiating the conversion sequence.

Integrate Input

During the first period, switch #4 is closed (all others open), applying the input potential to the buffer input. Since the amplifier offsets are stored on the auto-zero capacitor, the integrator's slope is determined solely by the input voltage. The input voltage is integrated for exactly 1000 counts, thus reaching an integrator output proportional to the integral of the input for a fixed time.

Integrate Reference

At the end of 1000 counts, switch #4 is opened, the polarity flip-flop is set, and the integrate reference period begins. Depending on the polarity, switch #5 or #6 is closed, connecting the buffer input to ground or $2V_{ref}$. This causes the integrator to ramp towards its quiescent (auto-zero) point with a slope proportional to $+V_{ref}$ or $-V_{ref}$. When the integrator crosses its quiescent auto-zero point, the comparator changes state, causing the zero crossing detector to generate a conversion complete signal which inhibits the clock and loads the logic information into the output latches. Switch #5 (or #6) is opened, switches #1, #2, and #3 are closed, and the system returns to a quiescent auto-zero mode, awaiting the next initiate conversion signal. If 2000 counts are received prior to zero crossing, an out-of-range signal is generated which sets the "out-of-range" output and resets the system.

Note 1: Internal reference out ≃ 1.8V, reference input = 1,000 volts for 1.999 volt scale and 100mV for 199.9mV scale.
Note 2: External components shown are suggested for 3 readings/sec.
Note 3: Parallel BCD outputs and other latched outputs are strobed at end of conversion and retain data until completion of next conversion.
Note 4: Start/Reset should remain Low during Auto-Zero. Conversion is initiated by a positive pulse on start pin. (minimum width 100nsec).
Note 5: Component values ±20% typ.

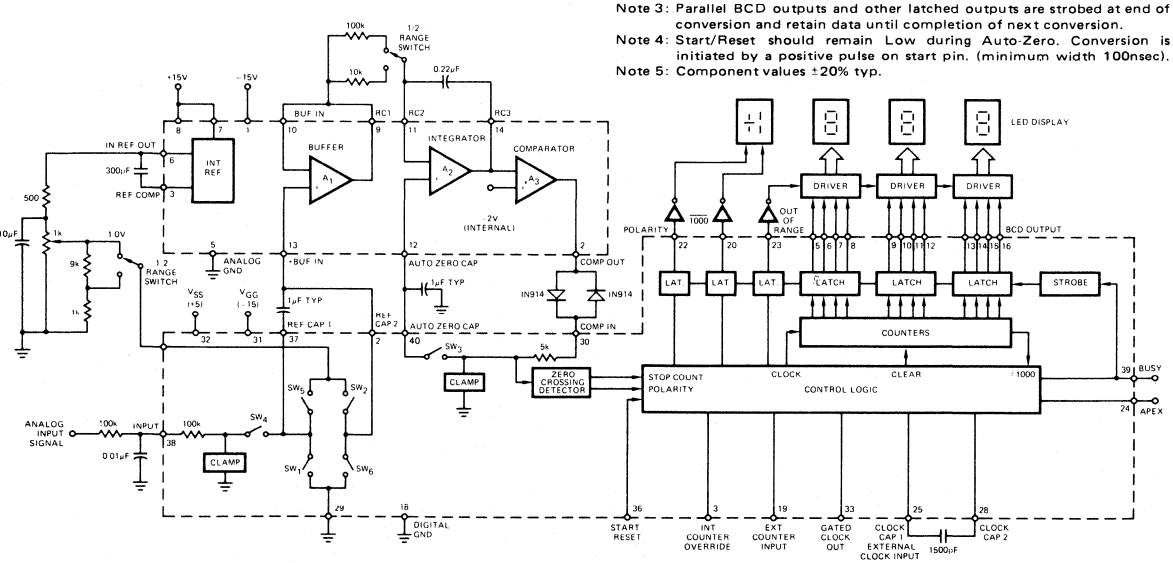


FIGURE 1. 3½ DIGIT A/D CONVERTER FUNCTIONAL DIAGRAM

7101 Digital Processor Controls

Two pins are included on the 7101 that allow the user to externally control the gain of the converter. The first pin, "Internal Counter Override", if held high, will inhibit the carry pulse from the internal counter that switches the converter from signal integrate to reference integrate. As long as this input is high, the converter will remain in the signal integrate mode. At the same time, it enables the other pin, External Counter Input, to supply this transition pulse from external sources. One technique for changing the gain of the system would be to hold "Internal Counter Override" high through the first N carry pulses. This would increase the signal integrate time by a factor of N+1 and, thus, the sensitivity of the system by N+1. Since the number of suppressed pulses could be controlled digitally, the system could accomodate signals from ±2.000V to ±200.0mV (or lower, if time permits) without changing the external analog scale factor components. By using more complex external logic and both inputs, the user could digitally set offset (tare) and scale factor to convert voltages to physical units such as "degrees centigrade", "pounds", or "feet".

A "BUSY" pin is provided which permits interrogating the 8052/7101 to determine the status of the conversion. During the signal integrate and reference integrate periods, the "busy" line is high until the conversion is complete, at which time "busy" line goes low. This transition can be used to signal "new data available".

The "Apex" pin provides a digital signal which goes high during the reference integrate period.

"OUT-OF-RANGE" is indicated by a latched "low" on pin 23 for counts over 2000. The BCD digital values are "high" (true), except $\overline{1000}$ which is "low".

A positive polarity of the analog input signal is indicated by a "high" state at the output of the "polarity" latch on pin 22.

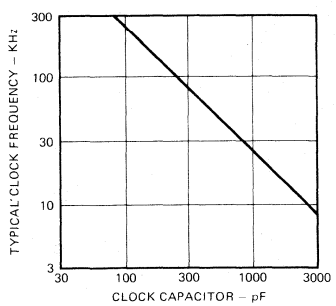


FIGURE 2.

The 7101 has an internal clock which requires a single capacitor between Pins 25 and 28 to operate. Figure 2 shows the typical capacitor value required to give the desired frequency.

During auto-zero, the clock is internally gated-off with Pin 28 high and Pin 25 low. When "start-reset" goes high, starting a measurement cycle, the clock starts counting with Pins 25 and 28 immediately changing phase. The counting continues until the end of the measurement cycle, at which time the clock is returned to its auto-zero condition.

In a typical application where visual readings are required, three readings per second is near the optimum speed. Faster readings make it difficult to resolve individual readings, while at slower rates the reader has to wait too long between measurements. In this application, 40% of the time (133mS) could be allocated to auto-zero and 60% (200mS) to signal and reference integrate. Since a measurement cycle consists of 3,000 clock pulses maximum, this dictates a clock frequency of 15kHz. Also, since the dual-slope technique of A/D conversion is not first-order dependent on clock frequency, the ±20% variation of clock frequency from unit-to-unit would result in no measurable error. However, in some applications, a more precise clock frequency would be desired. For instance, if precise rejection of 60Hz is required, the signal integrate phase (1,000 counts) would have to contain an integral number of 60Hz periods. For these applications, an external clock can be used by deleting the capacitor and connecting the external clock to Pin 25. However, if the clock is run asynchronously with start/reset, there will be one clock pulse of uncertainty in the integrate signal time, depending on where in the clock pulse period the start/reset went high. This will show up as one count of noise for signal near full-scale. This noise or jitter can be avoided by synchronizing the start/reset pulse to the negative-going edge of the external clock. Pin 33, Gated Clock Out, is a buffered output of the clock (internal or external) that is off (low) during auto-zero and in phase with Pin 25 during measurement.

Component Selection

Except for the reference voltage, none of the component values are first order important in determining the accuracy of the instrument. While this is undoubtedly an advantage of this approach, it does make the selection of nominal component values arbitrary at best. For instance, the reference capacitor and auto-zero capacitor are each shown as 1.0μfd. These relatively large values are selected to give greater immunity to PC board leakage since much smaller capacitors are adequate for charge injection errors or leakage errors from the 8052/7101.

The ratio of integrating resistor and capacitor is selected to give 9-volt swing for full-scale inputs. This is a compromise between possibly saturating the integrator (at ±14V) due to tolerance build-up between the resistor, capacitor, and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. Again, the .22μfd value for the integrating capacitor is selected for PC board considerations alone since the very small leakage at the integrator input is nulled at auto-zero. A very important characteristic of the integrating capacitor is low dielectric absorption. A polypropylene capacitor gave excellent results. In fact, a good test for dielectric absorption is to use the capacitor in this circuit with the input tied to reference. This ratiometric condition should read 1.000 and any deviation is probably due to dielectric absorption. In this ratiometric condition, a polycarbonate capacitor contributed an error of approximately 0.8 digit, polystyrene about 0.3 digit, and polypropylene less than 0.05 digit. The increased T.C. of polypropylene is of no consequence in this circuit. The dielectric absorption of the reference capacitor and auto-zero capacitor are only important at power on or when the circuit is recovering from an overload. Thus, smaller or cheaper capacitors can be used here if accurate readings are not required for the first few seconds of recovery.

The back-to-back diodes on the comparator output are recommended in the 200.0mV range to reduce the noise effects. In the normal operating mode, they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero capacitor. At start-up or recovery from an overload, their impedance is low to large signals so the capacitor can be charged in one auto-zero cycle. If only the 2.000V range is used, a 100k resistor in place of the back-to-back diodes is adequate for noise effects.

Maximum Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. Even though the comparator in this circuit is all NPN with an open loop gain-bandwidth product of 300MHz, it is no exception. The comparator output follows the integrator ramp with a 3μS delay. At a clock frequency of 160kHz (6μS period), half of the first reference integrate period is lost in delay. This means that the meter reading will change from 0 to 1 with 50μV in, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at mid-point is considered desirable by most users. However, if the clock frequency is increased appreciably above this, the instrument will flash 1 on noise peaks even when the input is shorted.

Some circuits use positive feedback or a latch to solve the delay problem. However, unless the comparator voltage swing, the comparator gain, and the integrator gain are carefully controlled, this circuit can generate **anticipation** errors that greatly exceed the 3μS **delay** error. Also, it is very susceptible to noise spikes. A more controlled approach for extending the conversion rate is the use of a small resistor in the integrator feedback loop. This feeds a small pulse to the comparator to get it moving quickly and partially compensate for its delay.

The minimum clock frequency is established by leakage on the auto-zero and reference capacitor. With most devices, measurement cycles as long as 10 seconds gave no measurable leakage error.

APPLICATIONS

8052/7101 3½ Digit LCD DPM/DVM

Figure 3 illustrates an application where the 8052/7101 interfaces with a Liquid Crystal Display. The CD4054 and CD4055s are Liquid Crystal Display Drivers (4-segment and 7-segment, respectively) which provide the level shifting (up to $30V_{p-p}$ at $V_{DD}-V_{EE}$ = 15V) necessary to drive the LCD. Overrange is indicated by a special character. If blanking of any part of the display is required on overload, Pin 23 (7101) can be used to drive Pin 7 on those display drivers via an inverter and level shift such as CD4009 or 74C903 or another CD4054. Display applications requiring a plus sign rather than a blank indication for positive analog input levels (i.e., +1.999 versus 1.999) need to invert the "polarity" logic output level which is normally high for positive analog input signals.

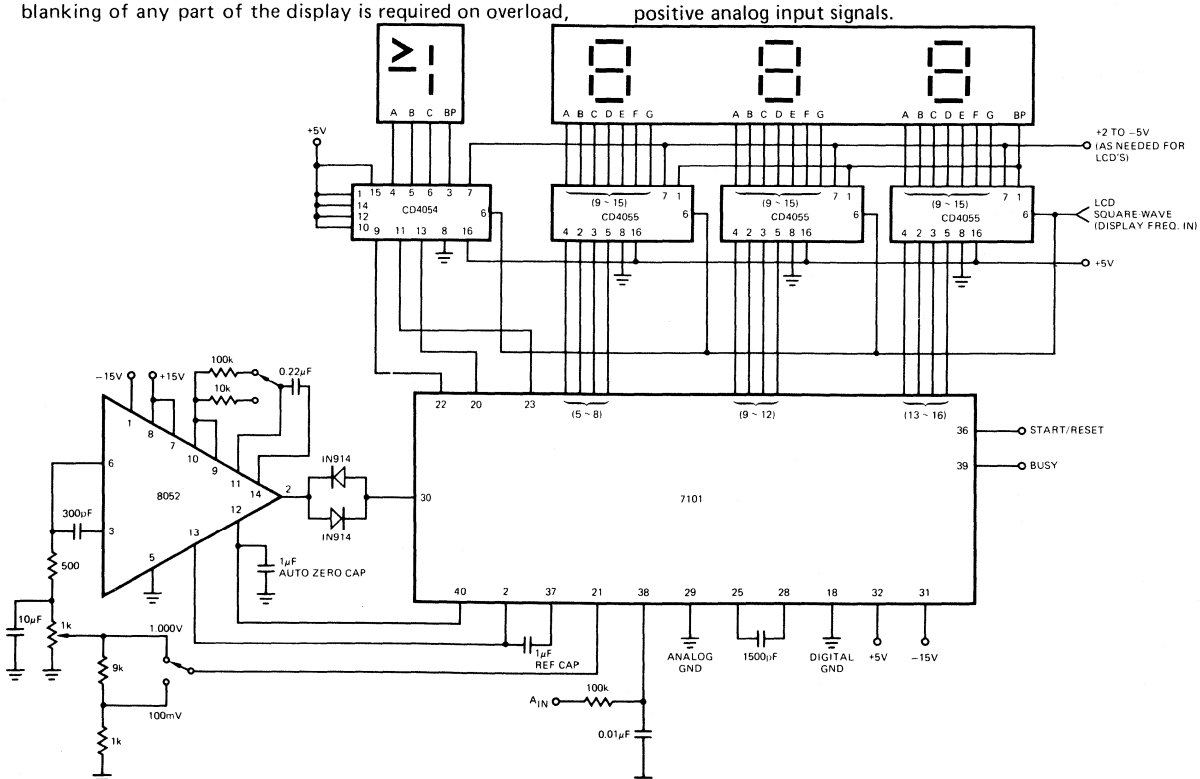


FIGURE 3. 8052/7101 3½ DIGIT LCD DPM/DVM

8052/7101/6100/6101 Set

The circuit in Figure 4 interfaces the 8052/7101 A-to-D converter chip set to an IM6100* microprocessor, using the 6101* Parallel Interface Element. Hex Tri-state Buffers (e.g., MM80C95*) are used to control bus access from the 7101 during read operations.

Conversion is initiated by activating the WRITE 1 line (positive going). The converter pair will then convert the analog input to digital form, and latch the data in the 7101. The busy line will go low as the conversion ends, and this transition is sensed by the SENSE 1 line, triggering an interrupt. The interrupt routine should read the 12-line data word, and then the polarity, $\overline{1000}$ and out-of-range lines.

Sufficient time must be allowed for the auto-zero loop to settle before retriggering a conversion. Ten milliseconds of auto-zero is sufficient to null any offsets to 10 microvolts. At power-on or after an overload, 100 milliseconds is required to assure the auto-zero capacitor has charged to the correct value. This time delay may be implemented conveniently using the IM6102 (Memory Extender/Time Delay Device).

Some skeletal service routines for this connection are given on page 7 and 8.

*References:
Intersil IM6100 CMOS 12-bit Microprocessor
Intersil IM6101 Parallel Interface Element
National MM80C95 Hex CMOS Tri-State Buffers

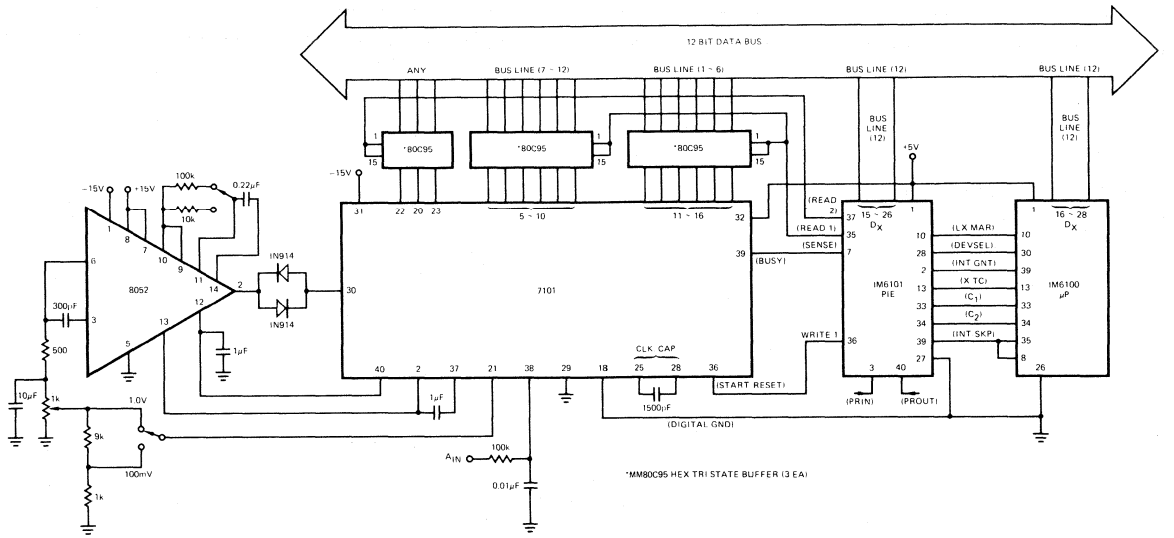


FIGURE 4. 3½ DIGIT PARALLEL BCD DATA ACQUISITION SYSTEM

8052/7101/6100/6101 APPLICATION PROGRAM

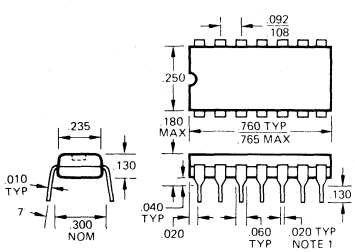
A possible set-up and service routine for the connection is given below.

```
/ASSUME PIE SELECT IS SET TO 54, INTERRUPT VECTOR TO 2000
        (OCTAL)
/INITIALIZE ROUTINE: SET-UP FOR NO INTERRUPT

1200    7200            CLA
1201    1240            TAD SSCRA
1202    6545            WCRA 54         /SET-UP CONTROL REGISTER A
1203    7200            CLA
1204    1241            TAD SSCRB
1205    6555            WCRB 54         /SET-UP CONTROL REGISTER B
1206    7200            CLA
1207    1242            TAD SSVV
1210    6556            WVR 54          /SET-UP VECTOR REGISTER

1220    0000  CONVERT,  Ø               /INITIATE CONVERSION SUBROUTINE
1221    1243            TAD SSCRAI
```

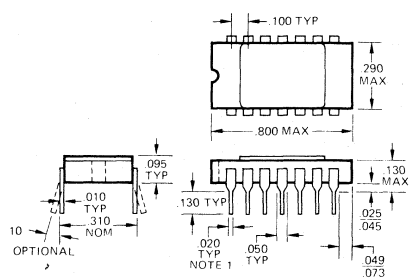
```
1222  6545          WCRA 54          /SET-UP CONTROL REGISTER A
1223  6541          WRITE1 54        /THE WRITE PULSE STARTS CONVERSION

1224  5620          JMP I CONVERT    /RETURN

1240  0040  SSCRA,  0040             /WP 1 SET HI, IE1 SET LO
1241  0000  SCRRB,  0000             /SL1, SP1 SET LP, NEGATIVE EDGE SENSE
1242  2000  SSVV,   2000             /VECTOR ADDRESS
1243  0041  SSCRAI, 0041             /WPI SET HI, IE1 SET HI

0000  0000  INTRPT, Ø                /ENTRY POINT FOR INTERRUPT
0001  6002          IOF              /DISABLE INTERRUPT, JUMP TO VECTOR ADDRESS

0140  0000  AD1,    Ø                /FIRST WORD OF DATA
0141  0000  AD2,    Ø                /SECOND WORD OF DATA
0160  0000  TEMP1,  Ø                /TEMPORARY STORAGE

2000  5210  VV,     JMP ATOD         /JUMP TO SERVICE POINT

2010  3160  ATOD,   DCA TEMP1        /SAVE AC
2011  6540          READ1 54         /READ BCD LINES
2012  3140          DCA AD1          /AND STORE
2013  6550          READ2 54         /READ POLARITY, 1000, AND OVERRANGE
2014  7040          CMA              /COMPLEMENT TO THE TRUE
2015  3141          DCA AD2          /AND STORE
/     – –   – – –   – – – –          /ANY OTHER WORK
2020  1160          TAD TEMP1        /RESTORE AC
2021  6001          ION              /RESTORE INTERRUPT
2022  5400          JMP I INTRPT     /RETURN
```

PACKAGE DIMENSIONS

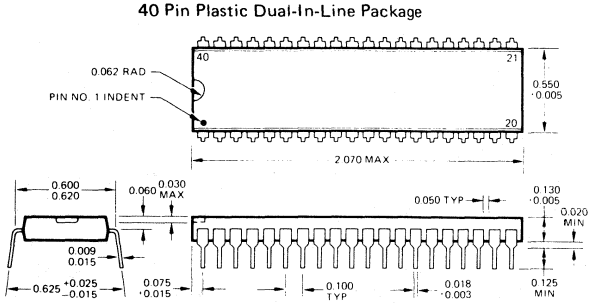
14 Pin Plastic Dual-In-Line Package



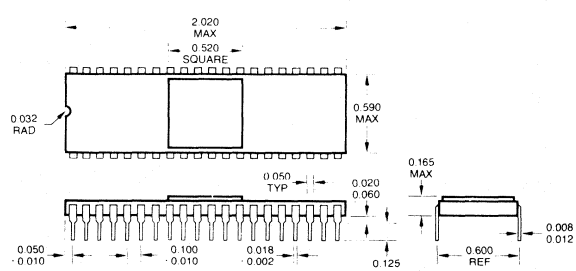
14 Pin Ceramic Dual-In-Line Package



40 Pin Plastic Dual-In-Line Package



40 Pin Ceramic Dual-In-Line Package



PRECISION PAIR FOR A-D CONVERTERS

4½ DIGIT PAIR 8052A/7103A
3½ DIGIT PAIR 8052/7103

FEATURES

- Accuracy guaranteed to ±1 count over entire ±20,000 counts (8052A/7103A)
- Guaranteed zero reading for 0 volts input
- 5pA input current typical
- True polarity at zero count for precise null detection
- Single reference voltage required
- Over-range and under-range signals available for auto-ranging capability
- All outputs TTL compatible
- Medium quality reference (40ppm typical) on board
- Blinking display gives visual indication of over-range
- Six auxillary inputs/outputs are available for interfacing to UARTS, Microprocessors or other complex circuitry

GENERAL DESCRIPTION

The 8052A/7103A with its multiplexed BCD outputs and digit drivers is ideally suited for the visual display DVM/DPM market. Accuracy is outstanding with performance like: 5pA input leakage, auto-zero to 10μV with less than 1μV/°C drift; linearity of 0.002%; scale factor temperature coefficients of 3ppm/°C (with external reference). The system uses the time-proven dual-slope integration with all its advantages, i.e., non-critical components, high rejection of noise and a-c signals, non-critical clock frequency, almost perfect differential linearity and true ratiometric readings. At the same time it has reduced or eliminated many of the sources of error that have limited dual-slope accuracy. With the 8052A/7103A pairs, critical board layout is no longer required to give low charge injection by the switches and elaborate ground planes are not necessary to keep clock pulse transients out of the comparator circuit.

The 8052/7103 (3½ digit pair) features conversion rates from 1 measurement every 10 seconds to 30/second, making them ideally suited for a wide variety of applications.

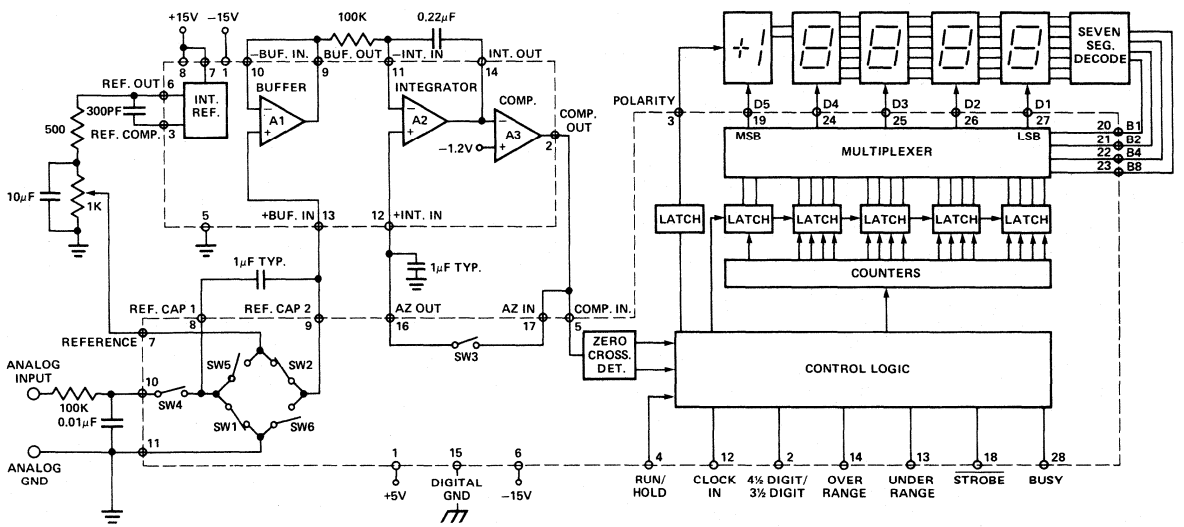


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

ORDERING INFORMATION

3½ Digit Pair

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to 70°C	14 pin ceramic DIP	ICL8052CDD
7103	0°C to 70°C	28 pin plastic DIP	ICL7103CPI
7103	0°C to 70°C	28 pin ceramic DIP	ICL7103CDI

4½ Digit Pair

Part	Temp. Range	Package	Order Number
8052A	0°C to 70°C	14 pin plastic DIP	ICL8052ACPD
8052A	0°C to 70°C	14 pin ceramic DIP	ICL8052ACDD
7103A	0°C to 70°C	28 pin plastic DIP	ICL7103ACPI
7103A	0°C to 70°C	28 pin ceramic DIP	ICL7103ACDI

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1)	500 mW
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 60 Sec.)	300°C

8052, 8052A

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration, All Outputs (Note 3)	Indefinite

7103, 7103A

Source Current (I_S)	100 mA
Drain Current (I_D)	100 mA
Digital Inputs	5 mA
V^+ to V^-	25V
Digital Input to V^+	V^- to V^+
Digital Input to V^-	V^+ to V^-

Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

SYSTEM ELECTRICAL CHARACTERISTICS

(V_{++} = +15V, V_+ = +5V, V_- = −15V Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	8052/7103(1)			8052A/7103A(2)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V Full Scale = 2.000V	−0.000	±0.000	+0.000	−0.0000	±0.0000	+0.0000	Digital Reading
Ratiometric Reading (3)	$V_{in} \equiv V_{Ref.}$ Full Scale = 2.000V	+0.999	+1.000	+1.001	+0.9999	+1.0000	+1.0001	Digital Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-2V \leqslant V_{in} \leqslant +2V$		0.2	1		0.5	1	Digital Count Error
Differential Linearity (difference between worse case step of adjacent counts and ideal step	$-2V \leqslant V_{in} \leqslant +2V$		.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 2V$		0.2	1		0.5	1	Digital Count Error
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 200.0mV Full scale = 2.000V		20 50			 30		μV
Leakage Current at Input	V_{in} = 0V		5	30		3	10	pA
Zero Reading Drift	V_{in} = 0V $0° \leqslant T_A \leqslant 70°C$		1	5		0.5	2	μV/°C
Scale Factor Temperature Coefficient	V_{in} = +2V $0 \leqslant T_A \leqslant 70°C$ (ext. ref. 0 ppm/°C)		3	15		2	5	ppm/°C

(1) Tested in 3½ digit (2,000 count) circuit shown in Fig. 3 clock frequency 12 kHz. Pin 2 7103 connected to Gnd.

(2) Tested in 4½ digit (20,000 count) circuit shown in Fig. 3 clock frequency 120 kHz. Pin 2 7103A open.

(3) Tested with a low dielectric absorbtion integrating capacitor. See Component Selection Section.

8052 ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8052			8052A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
EACH OPERATIONAL AMPLIFIER								
Input Offset Voltage	V_{CM} = 0V		20	50		20	50	mV
Input Current (either input)	V_{CM} = 0V		5	50		2	10	pA
Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio*	V_{CM} = ±2V		110			110		
Large Signal Voltage Gain	R_L = 10kΩ	20,000			20,000			V/V
Slew Rate			6			6		V/μs
Unity Gain Bandwidth			1			1		MHz
Output Short-Circuit Current			20	100		20	100	mA
COMPARATOR AMPLIFIER								
Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
Positive Output Voltage Swing		+12	+13		+12	+13		V
Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE								
Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
Output Resistance			5			5		ohms
Temperature Coefficient			50			40		ppm/°C
Supply Current Total			6	12		6	12	mA

*This is the only component that causes error in dual-slope converter.

7103 AND 7103A ELECTRICAL CHARACTERISTICS (V^+ = +5.0, V^- = −15V, Ta = 25°C)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUTS	Clock In, Run/Hold, 4½/3½	I_{inL} I_{inH}	V_{in} = 0 V_{in} = +5V		.2 .1	.6 10	mA μA
	Comp. In	I_{inL} I_{inH}	V_{in} = 0 V_{in} = +5V		.1 .1	10 10	μA μA
OUTPUTS	All Outputs	V_{OL}	I_{OL} = 1.6ma		.25	.40	V
	B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5	V_{OH}	I_{OH} = −1mA	2.4	4.2		V
	Busy, Strobe, Over-range, Under-range Polarity	V_{OH}	I_{OH} = −10μA	4.9	4.99		V
SWITCH	Switches 1, 3, 4, 5, 6	$R_{DS\ ON}$			400		Ω
	Switch 2	$R_{DS\ ON}$		1200			Ω
	Switch Leakage (All)	$I_{D\ OFF}$			2		pA
SUPPLY	+5V Supply Current	I_{CC}^+			20	30	mA
	−15V Supply Current	I_{CC}^-			4	6	mA

THEORY OF OPERATION

Figure 1 shows a function diagram for an A/D converter using the 8052/7103 pair. In this circuit, each measurement cycle is divided into four equal parts. The first part, phase 1, is the auto-zero cycle. The switch driver decoder recognizes this state and turns on hex switches number 1, 2, and 3. Switches 1 and 2 impress a voltage equal to V_{REF} across the reference capacitor. Switch 3 closes a loop around the integrator and comparator. The purpose of this loop is to charge up the auto-zero capacitor until the integrator output does not change with time. During the second part, Phase 2, switches 1, 2 and 3 are opened and switch 4 is closed. If the input voltage is zero, the buffer, integrator and comparator will see the same voltages that existed in the previous state. Thus, the integrator output will not change but will remain stationary during the entire signal-integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the auto-zero cycle and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this cycle, the sign of the ramp is latched into the polarity F/F. The final part, reference integrate, includes phases 3 & 4. The switch driver decoder uses the output of the polarity F/F in deciding whether to close switch 5 or 6. If the input signal was positive, switch 6 is closed and a voltage which is V_{REF} more negative than during auto-zero is impressed on the buffer input. If the input signal was negative switch 5 is closed and a voltage which is V_{REF} more positive than during auto-zero is impressed on the buffer input. Thus, the reference capacitor generates the equivalent of a (+) reference or a (—) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to zero. The time, or number of counts, required to do this is porportional to the input voltage. Since the reference cycle can be twice as long as the signal integrate cycle, the input voltage required to give a full scale reading $\equiv 2\ V_{REF}$. The circuit, as described to this point, is not new to this application. It has been used successfully for several years. However, this system makes three major contributions to the accuracy of this circuit. These are: (1) low charge injection, (2) junction FET op amp, and (3) zero-crossing flip-flop.

1. Low Charge Injection.

During auto-zero, there is no problem in charging the capacitors to the correct voltage. The problem is getting the switches off without changing this voltage. As the gate is driven off, the gate-to-drain capacitance of the switch injects a charge on the reference or auto-zero capacitor, changing its voltage. The designer, using discrete components, is forced into critical board layouts where charges of opposite polarity are injected to compensate or neutralize the driver injection. This balance will be upset by any unit-to-unit variation of switch capacitance so at best the final design is a compromise. In the 8052/7103 the critical layout has been done on the semiconductor chip and need not concern the user. Also, since a silicon-gate process is used for the switches, the unit-to-unit variation is extremely low. The net result is to give an error due to charge injection that is so low it is difficult to measure; but certainly less than 5μV referred to the input.

2. Junction FET Op Amps.

Both the buffer and integrator use junction FET inputs in a guarded circuit that reduces the voltage across the FET to 3 or 4 volts. At this voltage level, input leakage currents of 2 pA are typical. For typical component values 2 pA leakage contributes less than 2μV of error to the circuit. In theory, MOS FET's would contribute less leakage but their increased noise would more than swamp out any improvement.

3. Zero-Crossing Flip Flop.

The problem that the zero-crossing flip-flop is designed to solve is shown in figure 2.

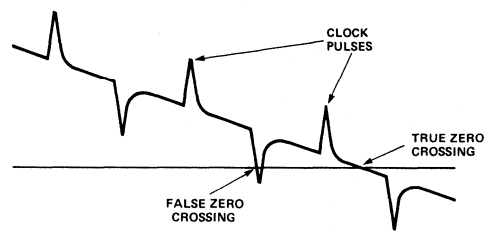


FIGURE 2. INTEGRATOR OUTPUT NEAR ZERO-CROSSING

The integrator output is approaching the zero-crossing point where the clock will be stopped and the reading displayed. The clock pulse feedthrough superimposed upon this ramp will cause a false reading by stopping the count prematurely. For a 20,000 count instrument, the ramp is changing approximately 0.50mV per clock pulse (10 volt max integrator output divided by 20,000 counts). The clock pulses have to be less than 100μV peak to avoid causing significant errors. The circuit layout to achieve this can be time consuming at best and impossible at worst. The suggested circuit gets around this problem by feeding the zero-crossing information into a flip-flop instead of using it directly. The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. Any false zero-crossing caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by one count in every instance. If a correction was not made, the display would always be one count too high. The correction is to disable the counter for one clock pulse at the beginning of phase 3. This one count delay compensates for the delay of the zero-crossing flip-flop and allows the correct number to be latched into the display. Similarly, a one count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2 so that true ratiometric readings are possible.

APPLICATIONS

Specific Circuits Using the 8052A/7103A

Figure 3 shows the complete circuit for a 4½ digit (±2.000V) full scale) A/D with LED readout using the internal reference of the 8052A. If an external reference is used, the reference supply (pin 7) should be connected to ground and the 300pF reference cap deleted. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower or the filter deleted completely. The ½ digit LED is driven off of the 7 segment decoder with a zero reading blanked by connecting a D5 signal to RBI input of the decoder.

A voltage translation network is connected between the comparator output of the 8052A and the auto-zero input of the 7103A. The purpose of this network is to assure that, during auto-zero, the output of the comparator is at or near the threshold of the 7103A logic (+2.5V) while the auto-cap is being charged to V_{REF} (+1.0 volts for a 2.000V instrument). Otherwise, even with zero volts in, some reference integrate period would be required to drive the comparator output to the threshold level. This would show up as an equivalent offset error. Once the divider network has been selected, the unit-to-unit variation should contribute less than a tenth of a count error. A second feature of the network is that it holds the source of switch 3 to ≈ +4V during the integrate and deintegrate cycles of positive input voltages. During this time, the comparator output is clamped by an internal diode on the 7103A to ≈ +5.7 volts. Since the gate of switch 3 is at +5 volts for this off condition, the +1 volt Vgs of the FET assures the switch is off to the 1 or 2 pA leakage level. Finally, the back-to-back diodes are used to lower noise. In the normal operating mode they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero cap. At startup or recovery from an overload, their impedance is low to large signals so that the cap can be charged up in one auto-zero cycle.

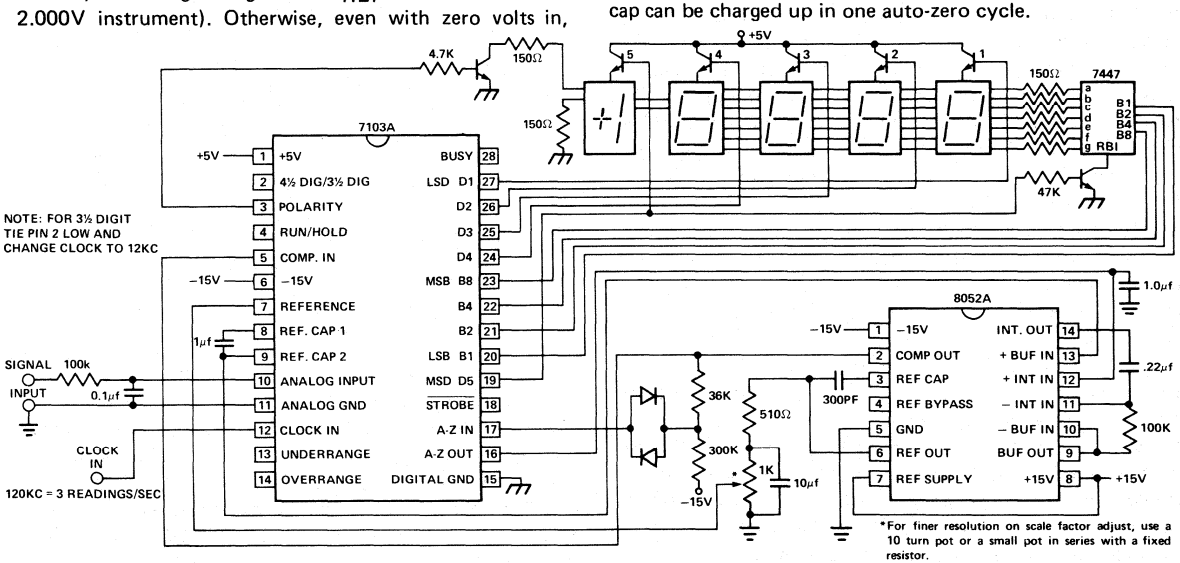


FIGURE 3. 8052A/7103A 4½ DIGIT A-D CONVERTER

Component Selection

Except for the Reference Voltage, none of the component values are first-order important in determining the accuracy of the instrument. While this is undoubtedly an advantage of this approach, it does make the selection of nominal component values arbitrary at best. For instance the reference capacitor and auto-zero capacitor are each shown as 1.0μF. These relative large values are selected to give greater immunity to PC board leakage since smaller capacitors are adequate for charge injection errors or leakage errors from the 8052/7103. The ratio of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at ±14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. Again the .22μF value for the integrating cap is selected for PC considerations alone since the very small leakage at the integrator input is nulled at auto-zero. A very important characteristic of the integrating cap is low dielectric absorption. A polypropylene cap gave excellent results in the application. In fact a good test for dielectric absorption is to test the subject cap in this circuit with the input tied to reference. This ratiometric condition should read 1.0000 and any deviation is probably due to dielectric absorption. In this test poly-carbonate caps typically read .9992, polystyrene, .9997 and polypropylene, 1.0000. The increased temperature coefficient of polypropylene is of no consequence in this circuit. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Max Clock Frequency

The maximum conversion rate of most dual-slope A-D converters is limited by the frequency response of the comparator. Even though the comparator in this circuit is all NPN with an open-loop gain-bandwidth product of 300MHz, it is no exception. The comparator output follows the integrator ramp with a 3μS delay. At a clock frequency of 160kHz (6μS period) half of the first reference integrate period is lost in delay. This means that the meter reading will change from 0 to 1 with 50μV in, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at midpoint is considered desirable by most users. However, if the clock frequency is increased appreciably above this, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, up to 500kHz clock rate may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The minimum clock frequency is established by leakage on the auto-zero and reference cap. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

AUXILIARY INPUTS/OUTPUTS

The 7103 and 7103A include several pins that allow them to operate conveniently in more sophisticated systems. These include:

1. 4½/3½ (Pin 2). When high (or open) the internal counter operates as a full 4½ decade counter with a complete measurement cycle requiring 40,000 counts. When held low, the least significant decade is cleared and the clock is fed directly into the next decade. A measurement cycle now requires only 4000 clock pulses. All 5 digit drivers are active in either case with each digit lasting 200 counts with pin 2 high (4½ digit) and 20 counts for pin 2 low (3½ digit). The only difference between 7103A and 7103 is that they were tested with this pin high and low respectively. Actually, most 7103 will operate satisfactorily in a 4½ digit application. They simply have not received the more complex testing required to prove it.

2. Run/Hold (Pin 4). When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,000/4,000 clock pulses. If taken low, the converter will continue the full measurement cycle that it is in and then hold this reading as long as pin 4 is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle beginning with 10,000/1,000 counts of auto zero. Of course if the pulse occurs before the full measurement cycle (40,000/4,000 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is in. An external indication that a full measurement cycle has been completed is that the first strobe pulse (see below) will occur 100/10 counts after the end of this cycle. Thus, if Run/Hold is low and has been low for at least 100/10 counts, the converter is holding and ready to start a new measurement when pulsed high.

3. $\overline{\text{Strobe}}$ (Pin 18). This is a negative going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative going $\overline{\text{Strobe}}$ pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 100/10 pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 200/20 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first $\overline{\text{Strobe}}$ pulse goes negative for ½ clock pulse width. Similarly, after 200/20 clock pulses, digit 4 goes high and 100/10 pulses later the $\overline{\text{Strobe}}$ goes negative for the second time. This continues through digit 1 (LSD) when the fifth and last $\overline{\text{Strobe}}$ pulse is sent. The digit drive will continue to scan (unless the previous signal was over-range) but no additional $\overline{\text{Strobe}}$ pulses will be sent until a new measurement is available.

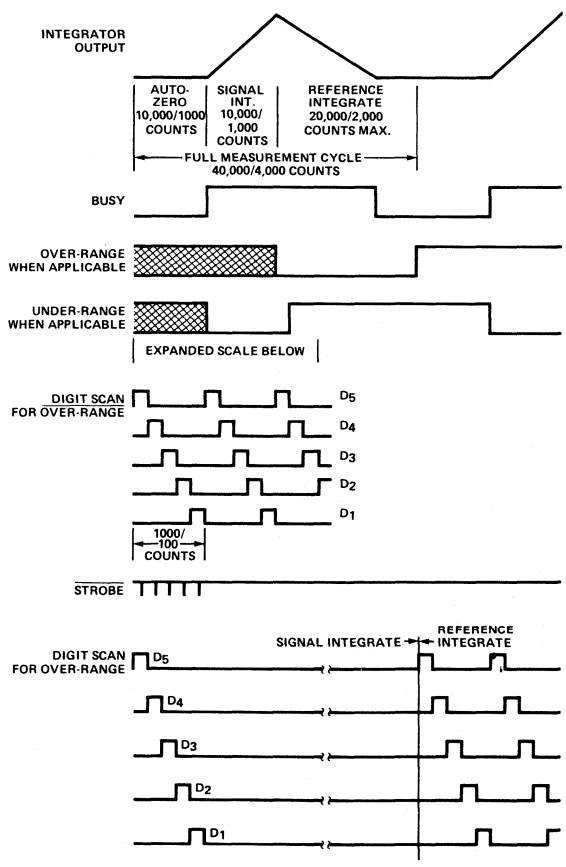


FIGURE 4. TIMING DIAGRAM

4. Busy (Pin 28). Busy goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an over-range). The internal latches are enabled (i.e., transferred during the first clock pulse after busy and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY so it may also be considered a $\overline{A\text{-}Z}$ signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001/1,001 counts from the number of pulses received (as mentioned previously there is one NO count pulse in each reference integrate (cycle).

5. Over-range (Pin 14). This pin goes positive when the input signal exceeds the range (20,000/2,000) of the converter. The output F-F is set at the end of Busy and is reset to zero at the beginning of Reference integrate in the next measurement cycle.

6. Under-range (Pin 13). This pin goes positive when the reading is 9% of range or less. The output F-F is set at the end of busy (if the new reading is 1800/180 or less) and is reset at the beginning of signal integrate of the next reading.

7. Polarity (Pin 3). This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal (+) and (—) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is re-validated for the next measurement.

8. Digit Drives (Pins 19, 24, 25, 26 and 27). The digit drives are a positive going signal that each last for 200/20 clock pulses. The scan sequence is D_5 (MSD), D_4, D_3, D_2 and D_1 (LSD). All five digits are scanned even when operating in the 3½ digit mode. The scan is continuous unless an over-range occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference Integrate when D_5 will start the scan again. This gives a blinking display as a visual indication of over-range.

9. BCD (pins 20, 21, 22 and 23). The Binary coded Decimal bits B_8, B_4, B_2 and B_1 are positive logic signals that go on simultaneously with the digit driver.

INTERFACING WITH UARTS AND MICROPROCESSORS

Figure 5 shows a very simple interface between a free-running 8052A/7103A and a UART. The five $\overline{\text{Strobe}}$ pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). If EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative.

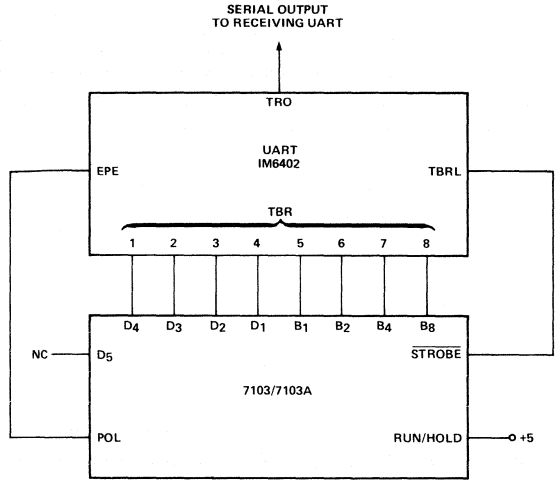


FIGURE 5. SIMPLE 7103/7103A TO UART INTERFACE

A more complex arrangement is shown in Fig. 6. Here the UART can instruct the A/D to begin a measurement sequence by a word on RRI. The Busy signal resets the Data Ready Reset (DRR). Again $\overline{\text{Strobe}}$ starts the transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D_5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

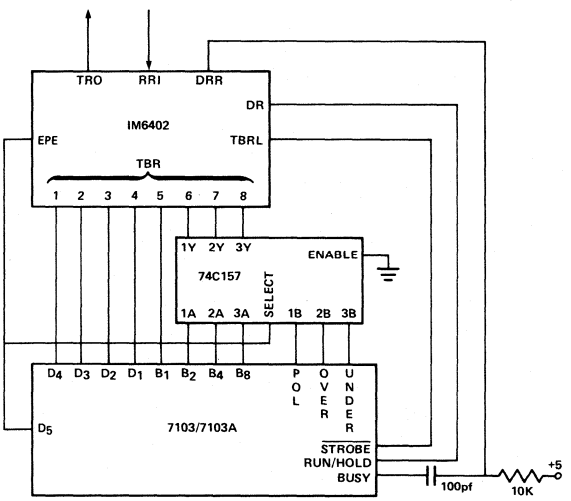


FIGURE 6. COMPLEX 7103/7103A TO UART INTERFACE

Circuits for the 7103/7103A to interface directly with three popular microprocessors are shown in Figures 7, 8 and 9. The main differences in the circuits are that IM6100 with its 12 bit word capability can accept polarity, over-range, under-range, 4 bits of BCD and 5 digits simultaneously where the 8080 and the MC6800 with 8 bits words need to have polarity, over-range and under-range multiplexed onto the Digit 5 word — as in the UART circuits. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

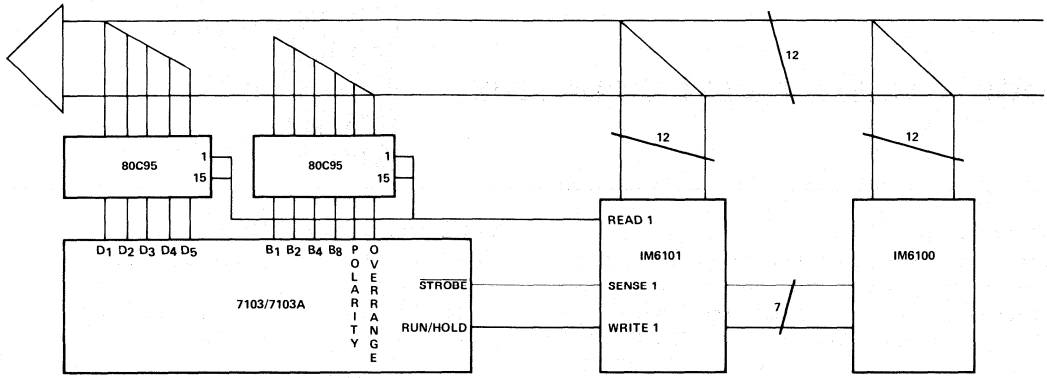


FIGURE 7. IM6100 TO 7103/7103A INTERFACE

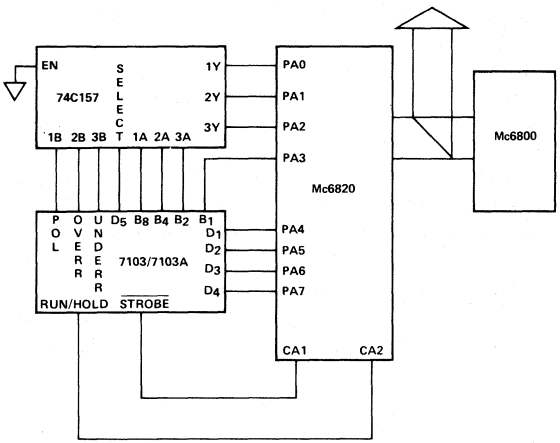


FIGURE 8. Mc6800 TO 7103/7103A INTERFACE

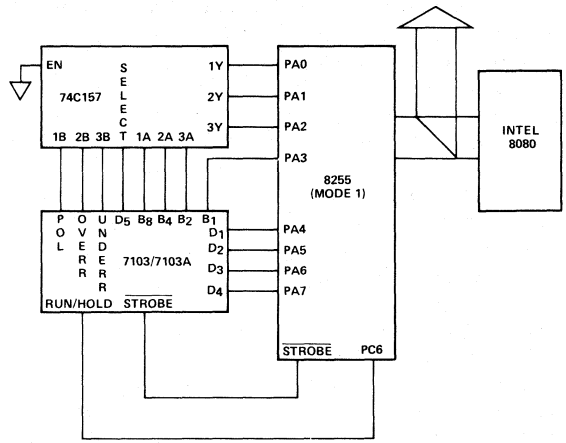
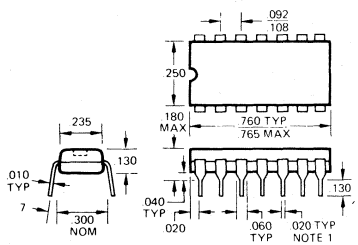


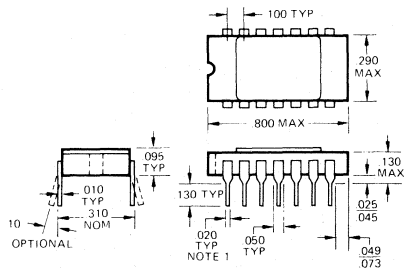
FIGURE 9. INTEL 8080 TO 7103/7103A INTERFACE

PACKAGE DIMENSIONS

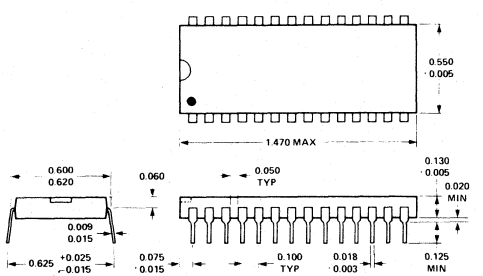
14 Pin Plastic Dual-In-Line Package



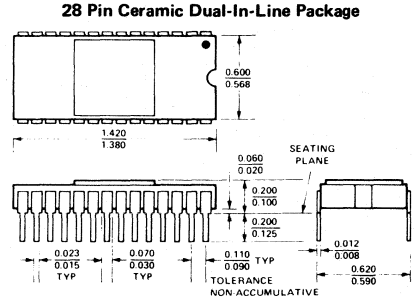
14 Pin Ceramic Dual-In-Line Package



28 Pin Plastic Dual-In-Line Package



28 Pin Ceramic Dual-In-Line Package



PROGRAMMABLE TIMERS/COUNTERS

Intersil 8240 8250 8260

FEATURES

- Times from microseconds to minutes, hours, or days
- Time base set by simple R, C network or external clock
- Programmable with standard thumbwheel switches
- Select output count from 1 RC to 255 RC (8240)
  1 RC to 99 RC (8250)
  1 RC to 59 RC (8260)
- Easily expanded to multiple decades (1 RC to 9,999 RC)
- Open collector outputs for flexibility
- High accuracy: ±0.5% typical
- Low drift: ±100ppm/°C typical
- Works over large supply range: 4V to 18V
- TTL compatible trigger and reset inputs

APPLICATIONS:

Programmable timing
- Process timers
- Appliance timers
- Darkroom timers

Programmable counter
- Inventory/loading/filling
- Counting/summing

Frequency generation
- Music synthesis
- Harmonic synchronization

Accurate, long-delay generator
A/D conversion
Digital Sample and Hold
Pattern generation

CONNECTION DIAGRAM

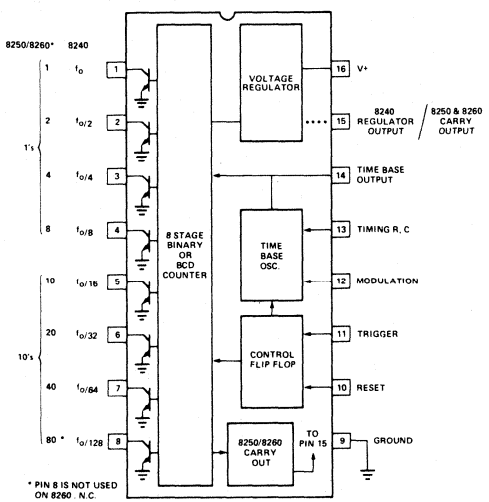


Figure 1.

GENERAL DESCRIPTION

The 8240, 8250 and 8260 are a family of monolithic programmable timer circuits. They are intended to simplify the problem of selecting various time delays or frequency outputs available from a fixed oscillator circuit.

Each device consists of an accurate, low-drift oscillator, a counter section of master-slave flip flops and appropriate logic and control circuitry all on one monolithic chip. The internal time base oscillator can be set with an external RC or can be disabled and the time base supplied from an external clock. The counter output taps are open collector transistors which can be programmed by a wire AND at external pins. Manual programming is easily accomplished by using standard thumbwheel switches. Additional logic circuitry will allow timing to be programmed by computer or microprocessor. These units are also very useful for generating ultra long delay times with relatively inexpensive RC components.

The 8260 is specifically designed to time accurate delays in seconds, minutes and hours. With its maximum count of 59 and carry out gate, a cascade of three 8260's will generate a one second clock from the 60 Hertz line, 60 seconds per minute and 60 minutes per hour programmable start to stop time. Thumbwheel switches with digits 0 to 5 and 0 to 9 are readily available to simplify the man-machine interface.

The 8250 is optimized for decimal counting and delays. It can be programmed by standard binary coded decimal (BCD) thumbwheel switches (0 to 9). Each unit gives 2 decades of counting allowing selection of time delays of from 1 RC to 99 RC. The carryout gate on the 8250 allows expansion to 9,999 or more.

The 8240 uses straight binary counting. With eight flip flops dividing down the base frequency, 8 suboctaves of the fundamental are available simultaneously in the astable mode. In the monostable mode the collectors can be wired AND to give any combination of pulse width of from 1 RC to 255 RC.

Applications for these versatile devices include appliance timers, darkroom timers and process timers. They can also be used as programmable counters. The internal clock can be disabled and the unit will count external pulses for programmable summing, loading or inventory applications. The internal clock can also be synchronized with the (m)th harmonic of an external sync and with the selectable counter, can provide a large number of non-harmonic frequencies from a single reference. Finally, they can be used as logic controlled switches in ramp type D-to-A and A-to-D converters.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V	Operating Temperature	
Power Dissipation		8240M, 8250M, 8260M	−55°C to +125°C
Ceramic Package	750 mW	8240C, 8250C, 8260C	0°C to +75°C
Derate above +25°C	6 mW/°C	Storage Temperature	−65°C to +150°C
Plastic Package	625 mW		
Derate above +25°C	5.0 mW/°C		

ELECTRICAL CHARACTERISTICS

8240

Test Conditions: See Figure 2, $V^+ = 5V$, $T_A = 25°C$, $R = 10k\Omega$, $C = 0.1\mu F$, unless otherwise noted.

PARAMETERS	8240M			8240C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
GENERAL CHARACTERISTICS								
Supply Voltage	4		18	4		18	V	For $V^+ < 4.5V$, Short Pin 15 to Pin 16
Supply Current								
Total Circuit (Reset)		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$. $V_{RS} = 5V$
Total Circuit (Trigger)		24			24			$V^+ = 15V$, $V_{TR} = 5V$, $V_{RS} = 0$ All outputs ON. (Worst Case)
Counter Only		1			1.5		mA	See Figure 3, 8240 only
Regulator Output, V_R	4.1	4.4		3.9	4.4		V	Measured at Pin 15, $V^+ = 5V$
(8240 only)	6.0	6.3	6.6	5.8	6.3	6.8	V	$V^+ = 15V$, See Figure 4
TIME BASE SECTION								See Figure 2
Timing Accuracy		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$, Note 1.
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ Over Operating Temperature
		80			80		ppm/°C	$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \geq 8$ Volts, See Figure 11
Max. Frequency	100	130			130		kHz	$R = 1\ k\Omega$. $C = 0.007\mu F$
Time Base Output								Measured at Pin 14
V_{TB} HIGH	2.4	2.8		2.4	2.8		V	$I_{Source} = 80\mu A$
V_{TB} LOW		0.2	0.4		0.2	0.4	V	$I_{Sink} = 3.2mA$
Modulation Voltage								Measured at Pin 12
Level	3.00	3.50	4.0	2.80	3.50	4.20	V	$V^+ = 5V$
		10.5			10.5		V	$V^+ = 15V$
Recommended Range of Timing Components								See Figure 8
Timing Resistor, R	0.001		10	0.001		10	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	
TRIGGER/RESET CONTROLS								
Trigger								Measured at Pin 11
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time		1			1		μsec.	Note 2
Reset								Measured at Pin 10
Reset Threshold		1.4	2.0		1.4	2.0	V	
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time		0.8			0.8		μsec.	Note 2
COUNTER SECTION								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.8	1.5			1.5		MHz	$V_{RS} = 0$, $V_{TR} = 5V$ Max Input to Pin 14
Input:								
Impedance		15			15		kΩ	Measured at Pin 14
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 1 thru 8
Rise Time		180			180		nsec.	$R_L = 3k$, $C_L = 10pf$
Fall Time		180			180		nsec.	
V_{OUT} Low		0.2	0.4		0.2	0.4	V	$I_{SINK} = 3.2$ mA
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} = 15V$

NOTE 1: Timing error solely introduced by 8240, measured as % of ideal time-base period of T = 1.00 RC.
NOTE 2: Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 2, $V^+ = 5V$, $T_A = 25°C$, R = 10 kΩ, C = 0.1 μF, unless otherwise noted.

PARAMETERS	8250M			8250C			UNITS	CONDITIONS
	MIN.	TYP.	MAX	MIN.	TYP.	MAX.		
GENERAL CHARACTERISTICS								
Supply Voltage	4.5		18	4.5		18	V	
Supply Current								
Total Circuit (Reset)		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
Total Circuit (Trigger)		24			24			$V^+ = 15V$, $V_{TR} = 5V$, $V_{RS} = 0$ All outputs ON. (Worst Case)
TIME BASE SECTION								See Figure 2
Timing Accuracy		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$, Note 1
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ Over Operating Temp.
		80			80		ppm/°C	$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \geqslant 8$ Volts, See Figure 11
Max. Frequency	100	130			130		kHz	R = 1 kΩ, C = 0.007 μF
Time Base Output								Measured at Pin 14
V_{TB} HIGH	2.4	2.8		2.4	2.8		V	$I_{SOURCE} = 80\mu A$
V_{TB} LOW		0.2	0.4		0.2	0.4	V	$I_{SINK} = 3.2mA$
Modulation Voltage								Measured at Pin 12
Level	3.00	3.50	4.0	2.80	3.50	4.20	V	$V^+ = 5V$
		10.5			10.5		V	$V^+ = 15V$
Recommended Range of Timing Components								See Figure 8
Timing Resistor, R	0.001		10	0.001		10	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	
TRIGGER/RESET CONTROLS								
Trigger								Measured at Pin 11
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time		1			1		μsec.	Note 2
Reset								
Reset Threshold		1.4	2.0		1.4	2.0	V	Measured at Pin 10
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time		0.8			0.8		μsec.	Note 2
COUNTER SECTION								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.8	1.5			1.5		MHz	$V_{RS} = 0$, $V_{TR} = 5V$ Max. Input Pin 14
Input:								
Inpedance		15			15		kΩ	Measured at Pin 14
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 1 thru 8
Rise Time		180			180		nsec.	$R_L = 3k$, $C_L = 10$ pF
Fall Time		180			180		nsec.	
V_{OUT} Low		0.2	0.4		0.2	0.4	V	$I_{SINK} = 3.2$ mA
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} = 15V$
CARRY OUT GATE								See Figure 4, $V^+ = 5V$
V_{CO} Low		0.2	0.4		0.2	0.4	V	Measured on Pin 15 $I_{SINK} = 3.2$ mA
V_{CO} High	2.4	3.5		2.4	3.5		V	$I_{SOURCE} = 80\mu A$

NOTE 1: Timing error solely introduced by 8250, measured as % of ideal time-base period of T = 1.00 RC.
NOTE 2: Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

ELECTRICAL CHARACTERISTICS

8260

Test Conditions: See Figure 2, $V^+ = 5V$, $T_A = 25°C$, R = 10 kΩ, C = 0.1 μF, unless otherwise noted.

PARAMETERS	8260M			8260C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
GENERAL CHARACTERISTICS								
Supply Voltage	4.5		18	4.5		18	V	
Supply Current								
Total Circuit (Reset)		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
Total Circuit (Trigger)		24			24			$V^+ = 15V$, $V_{TR} = 5V$, $V_{RS} = 0$
								All outputs ON. (Worst Case)
TIME BASE SECTION								See Figure 2
Timing Accuracy		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$, Note 1
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ Over Operating Temp.
		80			80		ppm/°C	$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \geqslant 8$ Volts, See Figure 11
Max. Frequency	100	130			130		kHz	R = 1 kΩ, C = 0.007 μF
Time Base Output								Measured at Pin 14
V_{TB} HIGH	2.4	2.8		2.4	2.8		V	$I_{Source} = 80\mu A$
V_{TB} LOW		0.2	0.4		0.2	0.4	V	$I_{Sink} = 3.2mA$
Modulation Voltage								Measured at Pin 12
Level	3.00	3.50	4.0	2.80	3.50	4.20	V	$V^+ = 5V$
		10.5			10.5		V	$V^+ = 15V$
Recommended Range of Timing Components								See Figure 8
Timing Resistor, R	0.001		10	0.001		10	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	
TRIGGER/RESET CONTROLS								
Trigger								Measured at Pin 11
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time		1			1		μsec.	Note 2
Reset								
Reset Threshold		1.4	2.0		1.4	2.0	V	Measured at Pin 10
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time		0.8			0.8		μsec.	Note 2
COUNTER SECTION								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.8	1.5			1.5		MHz	$V_{RS} = 0$, $V_{TR} = 5V$ Max Input Pin 14
Input:								
Impedance		20			20		kΩ	Measured at Pin 14
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 1 thru 7
Rise Time		180			180		nsec.	$R_L = 3k$, $C_L = 10$ pF
Fall Time		180			180		nsec.	
V_{OUT} Low		0.2	0.4		0.2	0.4	V	$I_{SINK} = 3.2$ mA
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} = 15V$
CARRY OUT GATE								See Figure 4, $V^+ = 5V$
V_{CO} Low		0.2	0.4		0.2	0.4	V	Measured on Pin 15
								$I_{SINK} = 3.2$ mA
V_{HIGH}	2.4	3.5		2.4	3.5		V	$I_{SOURCE} = 80\ \mu A$

NOTE 1: Timing error solely introduced by 8260, measured as % of ideal time-base period of T = 1.00 RC.
NOTE 2: Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

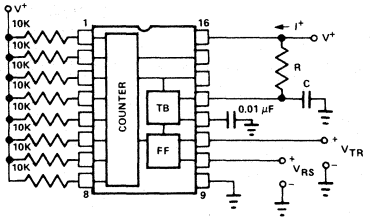


Figure 2. Generalized Test Circuit

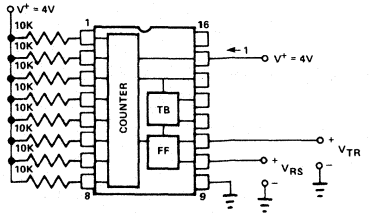


Figure 3. Test Circuit for Low-Power Operation (Time-Base Powered Down) 8240 Only.

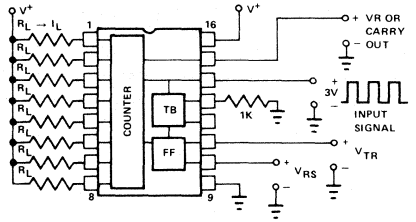


Figure 4. Test Circuit for Counter Section

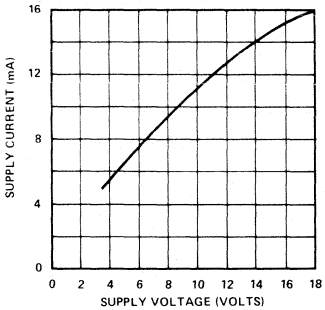


Figure 5. Supply Current vs. Supply Voltage in Reset Condition

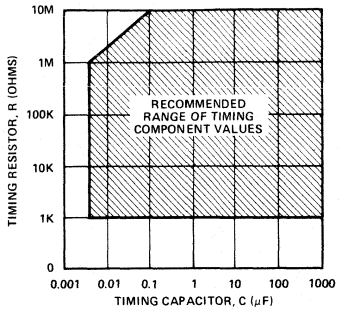


Figure 6. Recommended Range of Timing Component Values

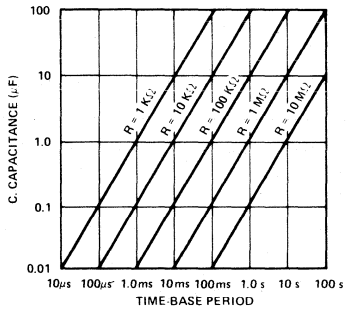


Figure 7. Time-Base Period, T, as a Function of External RC

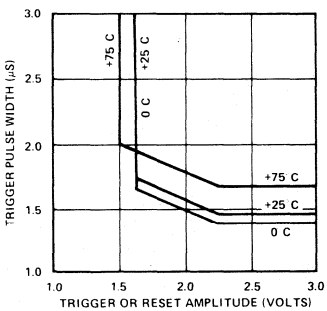


Figure 8. Minimum Trigger and Reset Pulse Widths at Pins 10 and 11

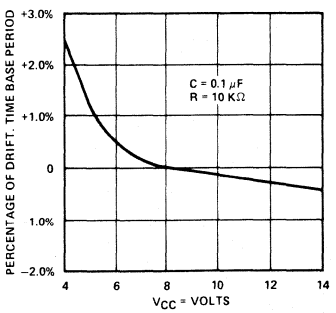


Figure 9. Power Supply Drift

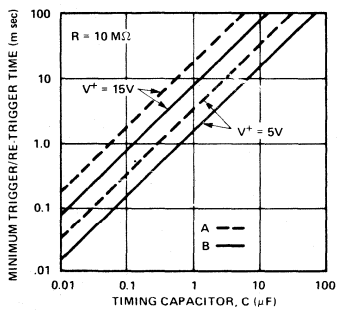


Figure 10.
A) Minimum Trigger Delay Time Subsequent to Application of Power
B) Minimum Re-trigger Time, Subsequent to a Reset Input

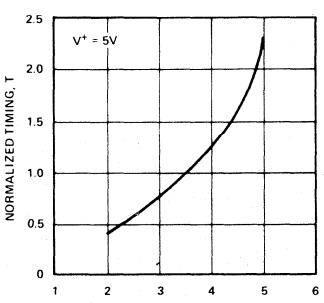


Figure 11. Normalized Change in Time-Base Period As a Function of Modulation Voltage at Pin 12

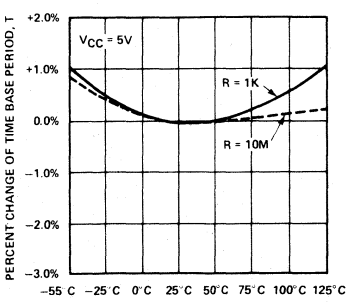


Figure 12. Temperature Stability at V_{CC} = 5V

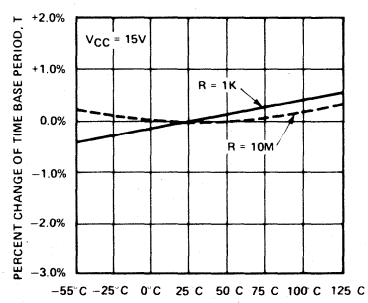


Figure 13. Temperature Stability at V_{CC} = 15V

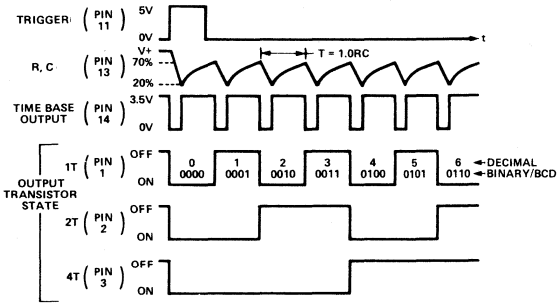


Figure 14. Timing Diagram of Output Waveforms (8240)
(Note: BCD States are not all symmetrical)

INTRODUCTION TO PROGRAMMABLE TIMING

A timing diagram of waveforms and circuit states is shown in Figure 14. A generalized circuit connection for the 8240/50/60 is shown is Figure 15.

The timing cycle is initiated by applying a positive-going trigger pulse to pin 11. This trigger pulse enables the counter section, sets all counter outputs to the "low" or "on" state, and starts the time base oscillator. Then external C is charged through external R from 20% to 70% of V+, generating a timing waveform with period, T, equal to 1 RC. A short negative clock or time base pulse occurs during the capacitor discharge portion of the waveform. (Normally this time is small compared with the period T but has been enlarged for Figure 14.) These clock pulses are counted by the binary counter of the 8240 or by a Binary Coded Decimal (BCD) Counter in the 8250/60. The timing cycle terminates when a positive-going reset pulse is applied to pin 10. When the circuit is at reset state, both the time base and the counter sections are disabled and all the counter outputs are at a "high" or "off" state. The carry-out is also high.

In most timing applications, one or more of the counter outputs are connected back to the reset terminal, as shown in Figure 15, with S_1 closed. In this manner, the circuit will start timing when a trigger is applied and will automatically reset itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the reset terminal (switch S_1 open), the circuit would operate in its astable or free-running mode, subsequent to a trigger input.

PROGRAMMING CAPABILITY

The counter outputs (pins 1 through 8) are open-collector type stages and can be shorted together to a common pull-up resistor to form a "wired-and" connection. The combined output will be "low" as long as any one of the outputs is low. In this manner, the time delays associated with each counter output can be *summed* by simply shorting them together to a common output bus as shown in Figure 15. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle. T_O, would be 32T for an 8240, and 20T for

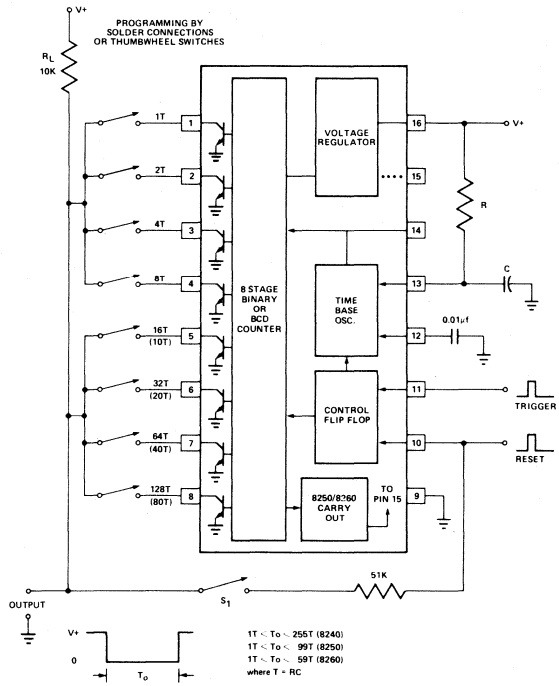


Figure 15. Generalized Circuit Connection for Timing Applications (Switch S_1 Open for Astable Operations, Closed for Monostable Operations)

an 8250. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be T_O = (1+16+32)T = 49T (8240) or (1+10+20)T = 31T (8250). In this manner, by proper choice of counter terminals connected to the outout bus, one can program the timing cycle to be:

$$1T \leqslant T_O \leqslant 255T \text{ (8240)}$$
$$1T \leqslant T_O \leqslant 99T \text{ (8250)}$$
$$1T \leqslant T_O \leqslant 59T \text{ (8260)}$$

Note that for the 8250 and 8260 invalid count states (BCD values $\geqslant$ 10) will not be recognized, and the counter will not stop.

THUMBWHEEL SWITCHES

While the 8240 is frequently hard wired for a particular function, the 8250 and 8260 can easily be programmed by using Thumbwheel switches. Standard BCD thumbwheel switches have four inputs (2^0, 2^1, 2^2, 2^3 or 1, 2, 4 and 8) and one "common", which are connected according to the binary equivalent of the digits 0 through 9.

For a single 8250 two such switches would select a time of from 01 RC to 99 RC. A cascade of two 8250's (using the carry out gate) would expand selection to 9999 RC. For an 8260 there are standard BCD Thumbwheel switches for the 0 through 5 digit (Twelve position, 0 to 5 repeated).

DESCRIPTION OF CIRCUIT CONTROLS

COUNTER OUTPUTS (PINS 1 THROUGH 8)

The binary counter outputs are buffered "open-collector" type stages, as shown in Figure 15. Each output is capable of sinking ≈ 5 mA of load current. At reset condition, all the counter outputs are at high or non-conducting state. Subsequent to a trigger input, the outputs change state in accordance with the timing diagram of Figure 14.

The counter outputs can be used individually, or can be connected together in a wired-and configuration, as described in the Programming section.

GROUND (PIN 9)

This is the return or most negative supply for the device. It should have a very low impedance since capacitor discharge and other switched currents could create transients.

RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11. The threshold level for these controls is approximately two diode drops (≈ 1.4V) above ground, and is therefore TTL/DTL compatible.

When power is applied to the 8240/50/60 with no trigger or reset inputs, the circuit reverts to "reset" state. Once triggered, the circuit is immune to additional trigger inputs, until the timing cycle is completed or a reset input is applied. If both the reset and the trigger controls are activated simultaneously, trigger overrides reset. Minimum pulse widths for reset and trigger inputs are shown in Figure 8.

MODULATION AND SYNC INPUT (PIN 12)

The period T of the time-base oscillator can be modulated by applying a dc voltage to this terminal (see Figure 11). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12, as shown in Figure 27. Recommended sync pulse widths and amplitudes are also given in the figure.

TIMING TERMINAL (PIN 13)

The time-base period T is determined by the external RC network connected to this pin. When the time-base is triggered, the waveform at pin 13 is an exponential ramp with a period T = 1.0 RC. Figures 5 and 6 show RC values.

TIME-BASE OUTPUT (PIN 14)

Time-Base output is an open-collector type stage, as shown in Figure 16. An internal 10kΩ pull-up resistor is provided to ensure correct operation. At reset state, the time-base output is at "high" state. Subsequent to triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of Figure 14.

Time-base output is internally connected to the binary counter section and also serves as the input for the external clock signal when the circuit is operated with an external time-base.

The counter input triggers on the negative-going edge of the timing or clock pulses applied to pin 14. The trigger threshold for the counter section is ≈ +1.4 volts. The counter section can be disabled by clamping the voltage level at pin 14 to ground.

Under certain operating conditions such as high supply voltages (V+ > 7V) and small values of timing capacitor (C < 0.1 μF) the pulse-width of the time-base output at pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 300 pF capacitor from pin 14 to ground.

CARRY OUTPUT (PIN 15, 8250 AND 8260 ONLY)

This pin will go HI for the last 10 counts of a 59 or 99 count, and can be used to drive another 8250 or 8260 counter stage, while still using all the counter outputs of the first. Thus, by cascading several 8250's a large BCD count-down can be achieved. The carry-out can also be used to drive TTL logic, etc.

REGULATOR OUTPUT (PIN 15, 8240 ONLY)

This terminal can serve as a V+ supply to additional 8240 circuits when several timer circuits are cascaded (see Figure 20), to minimize power dissipation. For circuit operation with external clock, pin 15 can be used as the V+ terminal to power-down the internal time-base and reduce power dissipation.

When the internal time-base is used with V+ ≤4.5V, pin 15 should be shorted to pin 16.

V+ (PIN 16)

This is the most positive supply voltage. (4.5V to 18V) A low supply impedance or 0.1μF to ground will help suppress voltage transients.

CIRCUIT OPERATION

A simplified schematic of the 8240 series devices is shown in Figure 16. The basic circuit waveforms and timing diagrams are shown in Figure 14. Probably the easiest way to understand the overall circuit operation is to consider each of the basic circuit elements separately. These are shown as blocks in the connection diagram of Figure 1.

The **Voltage Regulator,** for example, simply consists of a 7 volt zener diode, D1, biased by current source I_3 and buffered by NPN emitter follower Q10. Internally this regulator supplies power to all logic and counter stages. While all devices have regulators, only on the 8240 is the regulator output voltage brought out on Pin 15. In the 8250 and 8260 the Carry Output function is substituted at pin 15.

The **Oscillator Section** is composed of 2 comparators, an NPN pair, Q5 and Q6, and a PNP pair, Q7 and Q8, along with an Oscillator Flip Flop, Q15 and Q16. The reference voltage levels for the two comparators are determined by the resistor divider R1, R2 and R3 at the bases of Q6 and Q8. During the time the external resistor R is exponetially charging the external capacitor C at pin 13, both comparators are off as are Q2 and Q3. As the voltage on the external C approaches the upper reference level at pin 12, Q5 turns on, turning on PNP, Q4, setting the flip flop to the state with Q15 on and Q16 off. With the collector of Q16 high, Q18 turns on NPN's Q19 and Q3. Q3 very rapidly discharges the external capacitor towards the lower reference level on the base of Q8. As soon as the capacitor reaches this level Q7 turns on, turning on Q9 which resets the Oscillator Flip Flop to the state with Q15 off and Q16 on. Q16 turning on, turns off Q18 which turns off Q19 and Q3 completing the cycle. Note that Q3 and Q19 were on only for the discharge portion of the capacitor waveform. The collector of Q19 is then normally high going low during each discharge and returning to the high state. This short negative going pulse is used as the **Time Base** which drives the counter stages and is available at Pin 14.

The **Control Flip Flop,** transistors Q12 and Q13, is used to inhibit the oscillator circuitry during reset and forces a start at a discharge point when triggered. First consider the **reset condition,** i.e. Reset (pin 10) momentarily high and the Trigger (pin 11) always low. Reset high turns on Q14 resetting the Control Flip Flop to the state with Q12 off and Q13 on. This turns on Q20 which turns on Q1, Q17 and all the reset gates (R) at each counter stage (e.g., Q28). As long as Q17 is on, the discharge transistor Q3 will be held off, allowing the external capacitor to charge up.

During this reset state, PNP current source Q2 is turned on by Q1. This charges the external capacitor to nearly V+ turning on the upper comparator which is now ready to switch the Oscillator Flip Flop to the discharge mode as soon as Q17 is turned off.

The circuit state just described is the reset state. The Reset pin need only be high long enough to set the Control Flip Flop to the reset mode. The circuit will remain in this state until a high trigger pulse is received. Also notice that if neither a Trigger nor Reset input is present (high) when power is first supplied, the unbalanced collector load resistors of Q12 and Q13 will supply more base drive to Q13 and will force the Control Flip Flop to the reset state.

Now consider the case where the device has been in the reset state and the Trigger input is brought high. A high **Trigger input** turns on Q11 and sets the Control Flip Flop in the state with Q12 ON and Q13 OFF. This acts through Q20 to turn off Q1, Q17 and all the counter reset gates. As seen above, in reset, Q2 charged the external cap and turned on Q5 and Q4. Now as soon as Q17 goes off the Oscillator Flip Flop is set by the current from Q4 to the discharge mode with Q15 ON and Q16 OFF turning on the discharge transistor Q3. Again, the capacitor is rapidly discharged to the lower threshold level whereupon Q7 and Q9 turn on resetting the Oscillator Flip Flop to the charge mode.

This triggering scheme has several advantages. The most important is that the timing cycle of the first time base period is nearly identical to those that follow. This is because the capacitor discharge time is small compared to the exponential R, C charging time, and discharging from V+ rather than the upper threshold is usually a negligible timing error. This trigger scheme also generates an initial time base pulse (recall that Pin 14 goes low during discharge). This pulse clocks the counter stage to start the count at zero.

Let us now examine one of **the Counter Flip Flops** used in the eight binary counting stages. The first flip flop shown in detail is essentially Q26 and Q27 with steering or memory elements Q24 and Q25 being clocked by Q23. Q and $\overline{Q}$ outputs are taken from followers Q22 and Q29 with a reset input at Q28. Starting with the reset state, a high at pin 10 will set the Control Flip Flop such that Q28 and all other reset gates are turned on. This resets the counter flip flop with Q26 on and Q27 off. With Q26 on, Q22 will be off and the first stage output transistor T_1 will also be off. If a collector pull up resistor is connected to pin 1, the output will be high. Projecting this to successive stages, when Q26 (or its equivalent) is on in any counter stage Q22 and T_1, the output transistor, (or its equivalent) are turned off. When Q26 (or its equivalent) is off in any counter stage that output transistors will be turned on and the output will be low.

The toggle input to the flip flop comes in to the base of Q23. (The extra diode D6 sets the toggle threshold at 2 V_{be} as in TTL). In the first of the counter stages the input is driven from the Time Base Output (the collector of Q19 at Pin 14). In the reset state the time base is high which turns on Q23. When a trigger pulse is applied at pin 11 two things happen. First, the Control Flip Flop goes to the trigger state which removes the force voltage from

all flip flop reset transistors such as Q28. (This will not change the state of the flip flops but will allow them to respond to changes at the Toggle input). Second, the time base output goes low (recall the external cap is being discharged briefly). This turns off Q23 and allows its collector to go high. As the collector of Q23 goes high one of the "memory" elements (here Q24) pumps base current into the off side of the flip flop (Q27) causing the flip flop to change state (in this case with Q27 on and Q26 off). In this way the toggle input causes the first flip flop to change state at each time base negative going pulse. The second flip flop, being driven from the first, toggles when Q27 goes low and every other time base pulse thereafter and so on down the counter chain. Notice that at the first time base pulse (i.e., due to a trigger input after reset) all the flip flops ripple through and toggle from the Output High state to Output Low. They then begin their straight binary or BCD counting of subsequent time base pulses. The BCD counters include special gating on some flip flops.

The last logic element on the schematic is the **Carry Out Gate** for the 8250 and 8260. Transistors Q32 and Q33 form a NAND gate being driven from the last flip flop (The 80 digit/8250) (the 40 digit/8260) and the fifth flip flop (the 10 digit). Therefore pin 15 goes low after a Trigger and goes high only for the last 10 counts of a 99 or 59 count. Pin 15 goes low again (driving the time base input to the next cascaded unit) at a count of 100 and 60 respectively.

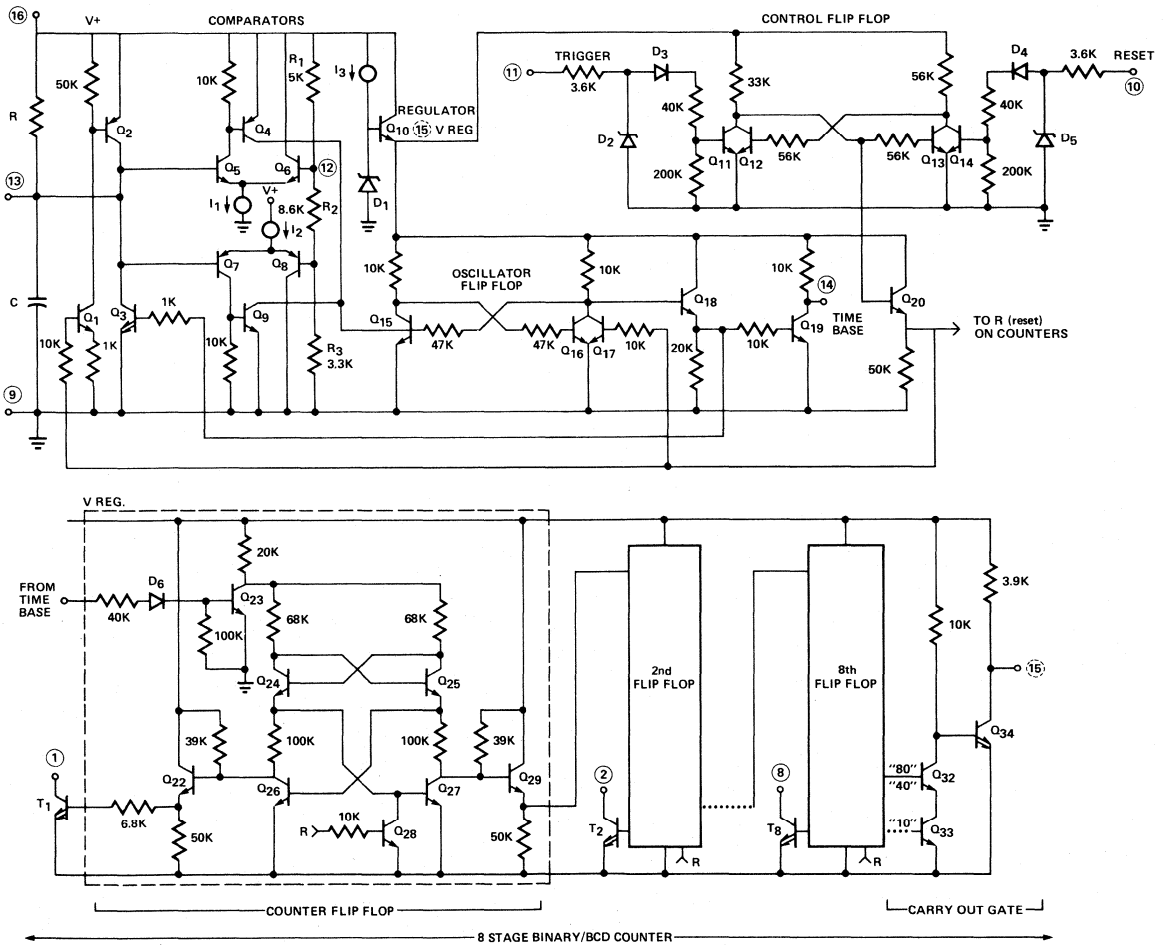


Figure 16. Equivalent Circuit

APPLICATIONS INFORMATION

PRECISION TIMING (Monostable Operation)

In precision timing applications, the 8240/50 is used in its monostable or "self-resetting" mode. The generalized circuit connection for this application is shown in Figure 17.

The output is normally "high" and goes to "low" subsequent to a trigger input. It stays low for the time duration T_O and then returns to the high state. The duration of the timing cycle T_O is given as:

$$T_O = NT = NRC$$

where $T = RC$ is the time-base period as set by the choice of timing components at pin 13 (see Figure 7). N is an integer in the range of:

$$1 \leqslant N \leqslant 255\ (8240) \leqslant 99\ (8250) \leqslant 59\ (8260)$$

as determined by the combination of counter outputs (pins 1 through 8) connected to the output bus, as described before. (see page 6)

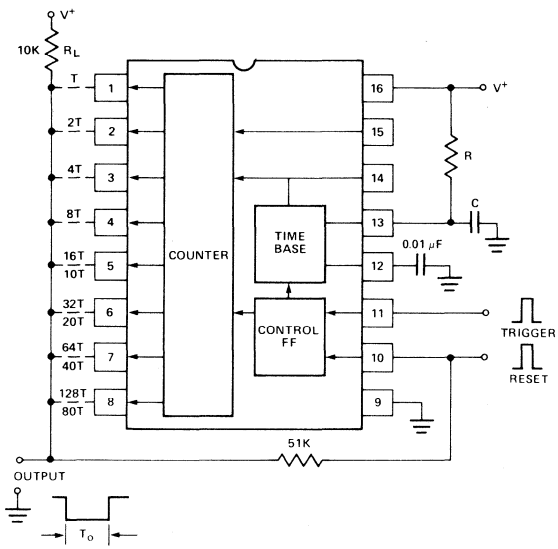


Figure 17. Circuit for Monostable Operation

ULTRA-LONG DELAY GENERATION

Two 8240/50/60 units can be cascaded as shown in Figure 18 to generate extremely long time delays. In this application, the reset and the trigger terminals of both units are tied together and the time base of Unit 2 disabled. In this manner, the output would normally be high when the system is at reset. Upon application of a trigger input, the output would go to a low state and stay that way for a total of $(256)^2$ or 65,536 cycles of the time-base oscillator (8240) or $(100)^2$ or 10,000 cycles (8250). The 8250/60 can also be connected as shown in Figure 19, allowing finer resolution in timing interval. The same applies to the 8260.

PROGRAMMING: Total timing cycle of two cascaded 8240's can be programmed from $T_O = 256RD$ to $T_O = 65{,}536RC$ in 256 discrete steps by selectively shorting any one or the combination of the counter outputs from Unit 2 to the output bus. Two cascaded 8250's can be programmed from $T_O = 1RC$ to $T_O = 9999RC$ in 10,000 discrete steps by selectively shorting any combination of the counter outputs from both units to the output bus.

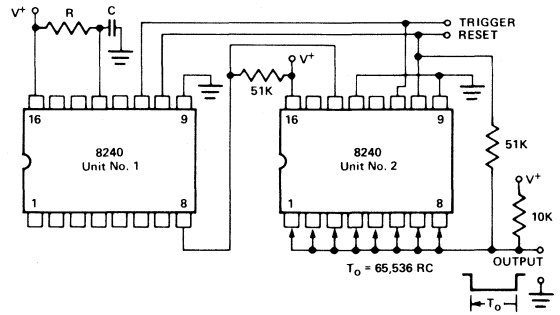


Figure 18. Cascaded Operation for Long Delay Generation (8240)

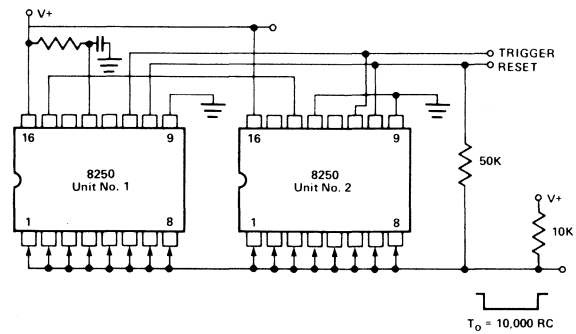


Figure 19. Cascaded Operation (8250 or 8260)

LOW-POWER OPERATION (8240 ONLY)

In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption, by using the circuit connection of Figure 20. In this case, the V+ terminal (pin 16) of Unit 2 is left open-circuited, and the second unit is powered from the regulator output of Unit 1, by connecting pin 15 of both units. The V+ terminal of an 8250 can be connected to pin 15 of an 8240, but the power drain is not greatly reduced by this connection.

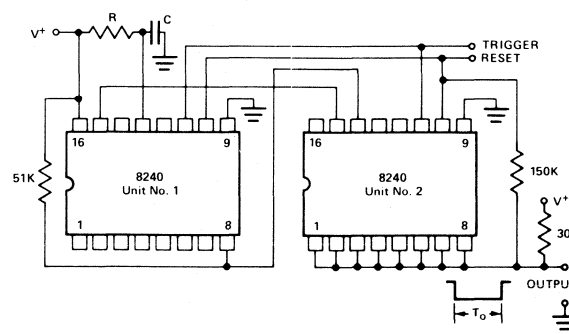


Figure 20. Low-Power Operation of Cascaded Timers (8240 only)

ELECTRONICALLY PROGRAMMED TIMER/COUNTER

The current interest in microprocessors, ROM's, PROM's, etc., requires timers which can be programmed electronically. Figures 21A and B show two ways of using readily available TTL/MSI logic to accomplish this. Although one is shown as a timer and the other as a counter, the choice of an external or internal clock would allow either circuit to perform either function.

The circuit of Figure 21A uses a standard 54/74 series TTL four bit magnitude comparator to compare the digitally programmed input with the 8240/50/60 counter outputs. The Greater, Less Than and Equal waveforms provide several outputs to choose from. An external start pulse triggers the timer and the A < B output is used as a reset.

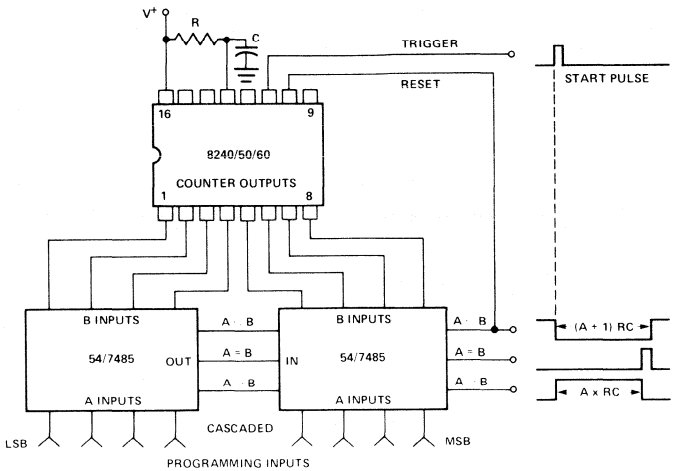


Figure 21A. Electronically Programmed Timer

In Figure 21B two Quad Exclusive Nor circuits with open collector outputs are wired together to form an inexpensive digital comparator. A start pulse triggers the 8240/50/60 counter and sets the output flip flop high. The digital comparator output goes high momentarily when A = B. This resets the flip flop which in turn resets the counter.

For extended temperature range or higher speed operation, individual pull-up resistors may be needed on the counter outputs of both circuits 21A and 21B.

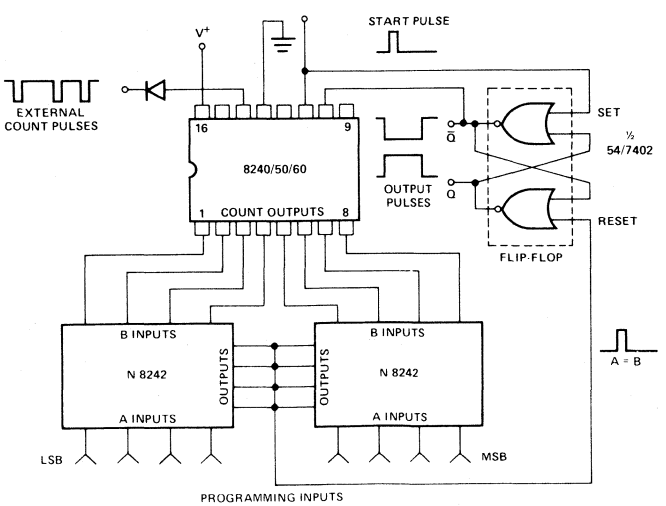


Figure 21B. Electronically Programmed Counter

ASTABLE OPERATION

The 8240/50 can be operated in its astable or free-running mode by disconnecting the reset terminal (pin 10) from the counter outputs. Two typical circuit connections for this mode of operation are shown in Figure 22. In the circuit connection of Figure 22(a), the circuit operates in its free-running mode, with external trigger and reset signals. It will start counting and timing subsequent to a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 10, the circuit reverts back to its rest state. The circuit of Figure 22(a) is essentially the same as that of Figure 15, with the feedback switch S_1 open.

The circuit of Figure 22(b) is designed for continuous operation. The circuit self-triggers automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely.

In astable or free-running operation, each of the counter outputs can be used individually as synchronized oscillators; or they can be interconnected to generate complex pulse patterns.

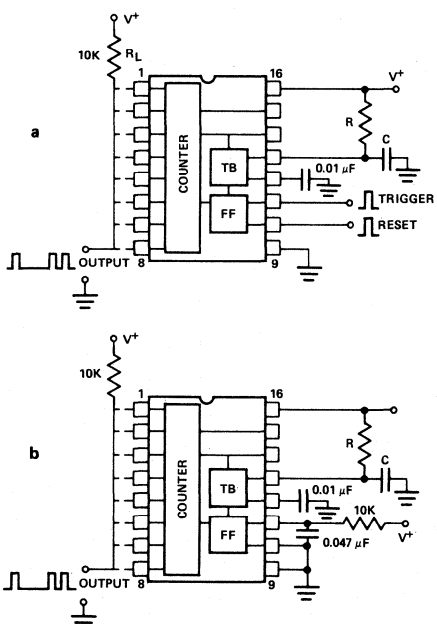


Figure 22. Circuit Connections for Astable Operation
(a) Operation with External Trigger and Reset Controls
(b) Free-running or Continuous Operation

BINARY OR DECIMAL PATTERN GENERATION

In astable operation, as shown in Figure 22, the output of the 8240/50 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 14 which shows the phase relations between the counter outputs. Figure 23 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the *highest* counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the *lowest* counter bit connected to the output.

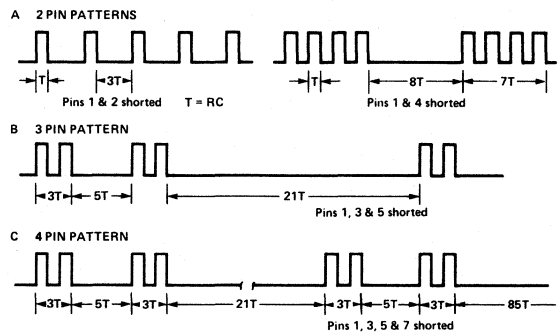


Figure 23. Pulse Patterns Obtained by Shorting Various Counter Outputs (Shown for the 8240)

OPERATION WITH EXTERNAL CLOCK

The 8240/50 can be operated with an external clock or time-base, by disabling the internal time-base oscillator and applying the external clock input to pin 14. The recommended circuit connection for this application is shown in Figure 24. The internal time-base can be de-activated by connecting pin 13 to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 volts is required. Minimum external clock pulse width is 1μs.

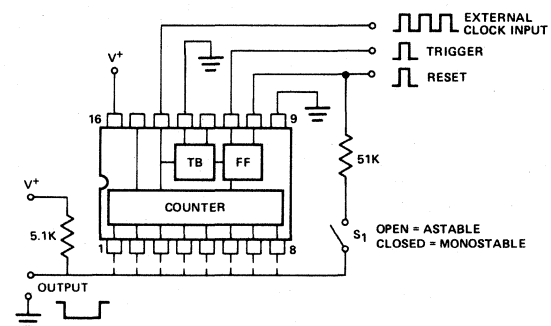


Figure 24. Operation with External Clock

FREQUENCY SYNTHESIZER

The programmable counter section of 8240/50 can be used to generate many discrete frequencies from a given time base setting using the circuit connection of Figure 25. The output of the circuit is a positive pulse train with a pulse width equal to T, and a period equal to (N+1) T where N is the programmed count in the counter.

The modulus N is the *total count* corresponding to the counter outputs connected to the output bus. Thus, for example, if pins 1, 3 and 6 are connected together to the output bus, the total count is: N = 1+4+32 = 37 and the period of the output waveform is equal to (N+1) T or 38T (25T for 8250). In this manner, many different frequencies can be synthesized from a given time-base setting.

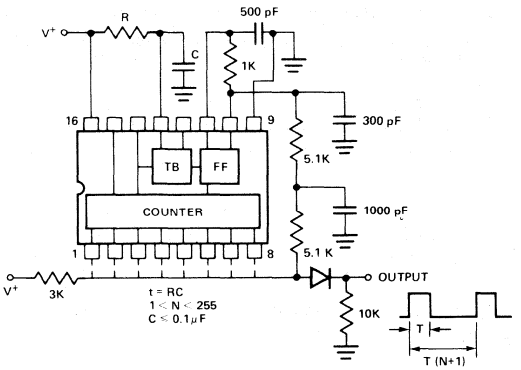


Figure 25. Frequency Synthesis from Internal Time-Base

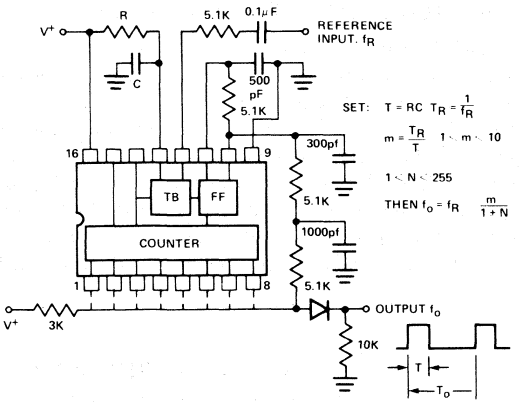


Figure 26. Frequency Synthesis by Harmonic Locking to an External Reference

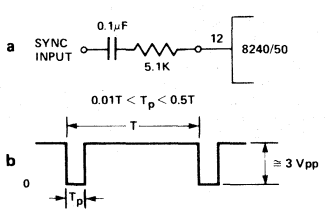


Figure 27. Operation with External Sync Signal.
(a) Circuit for Sync Input
(b) Recommended Sync Waveform

HARMONIC SYNCHRONIZATION

The time-base can by synchronized with *integer multiples or harmonics* of an input sync frequency, by setting the time-base period, T, to be an integer multiple of the sync pulse period, T_S. This can be done by choosing the timing components R and C at pin 13 such that:

$$T = RC = (T_S/m) \text{ where}$$
$$m \text{ is an integer, } 1 \leqslant m \leqslant 10.$$

Figure 28 gives the typical pull-in range for harmonic synchronixation, for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of time-base frequency. For $m > 10$, the circuit is too sensitive for reliable synchronization.

SYNTHESIS WITH HARMONIC LOCKING: The harmonic synchronization property of the 8240/50 time-base can be used to generate a wide number of discrete frequencies from a given input reference frequency. The circuit connection for this application is shown in Figure 26. (See Figures 27 and 28 for external sync waveform and harmonic capture range.) If the time base is synchronized to $(m)^{th}$ harmonic of input frequency where $1 \leqslant m \leqslant 10$, as described in the section on "Harmonic Synchronization", the frequency of f_o of the output waveform in Figure 26 is related to the input reference frequency f_R as:

$$f_o = f_R \frac{m}{(N+1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of $1 \leqslant N \leqslant 255$, the circuit of Figure 20 can produce 2550 different frequencies from a single fixed reference.

One particular application of the circuit of Figure 26 is generating frequencies which are not harmonically related to a reference input. For example, by choosing the external RC to set m = 10 and setting N = 5, one can obtain a 100 Hz output frequency synchronized to 60 Hz power line frequency. See Figure 30.

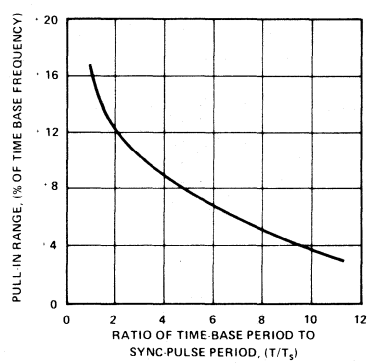


Figure 28. Typical Pull-In Range for Harmonic Synchronization

8260 APPLICATIONS

The 8260 provides a convenient method of generating accurate long delays where the inputs are programmed in terms of seconds, minutes and hours. An example of this is the 100 hour timer shown in Fig. 29. The 8260 on the right uses the carryout gate to generate a one second clock from a 60 hertz line source. The diodes on the time base input rectify the input signal and alternately clamp and release the internal pull up resistor at pin 14. The input network depends on the amplitude of 60 Hertz signal available. The internal oscillators are disabled with a 1K resistor to ground at pin 13.

The second and third 8260's are programmable with thumbwheel switches up to 59 seconds and 59 minutes. The carryout of each divider drives the next counter. An 8250 was chosen as the final stage to give a maximum count of 99 hours. All Reset pins are tied together and back to the 10K output pull up at the thumbwheel switches. The timing cycle begins by closing the push button to pulse the trigger inputs which are also tied together. The output is a normally high voltage which goes low when triggered. The output will stay low until the counters reach the time programmed at the thumbwheel switches. At that time the output returns to the high state and resets all the counters.

Some applications require monitoring of the continuing count. The Intersil ICM 7045 (or 7208) provides a counter chip plus direct drive to seven segment LED displays. The counter can be reset from the 8260 (or 8250) timer after the programmed count is reached.

The timing resolution can be increased to hundreths of a second by substituting 8250's for the initial stages and using the 60 Hertz line to generate a 100 Hertz clock. This was shown in Figure 26 under synthesis with harmonic locking. See Figure 30.

For applications with no 60 Hertz signal available the Intersil ICM7049 is recommended. This part works with a 4Mhz quartz crystal to generate a very stable one pulse per second clock frequency. See Figure 31.

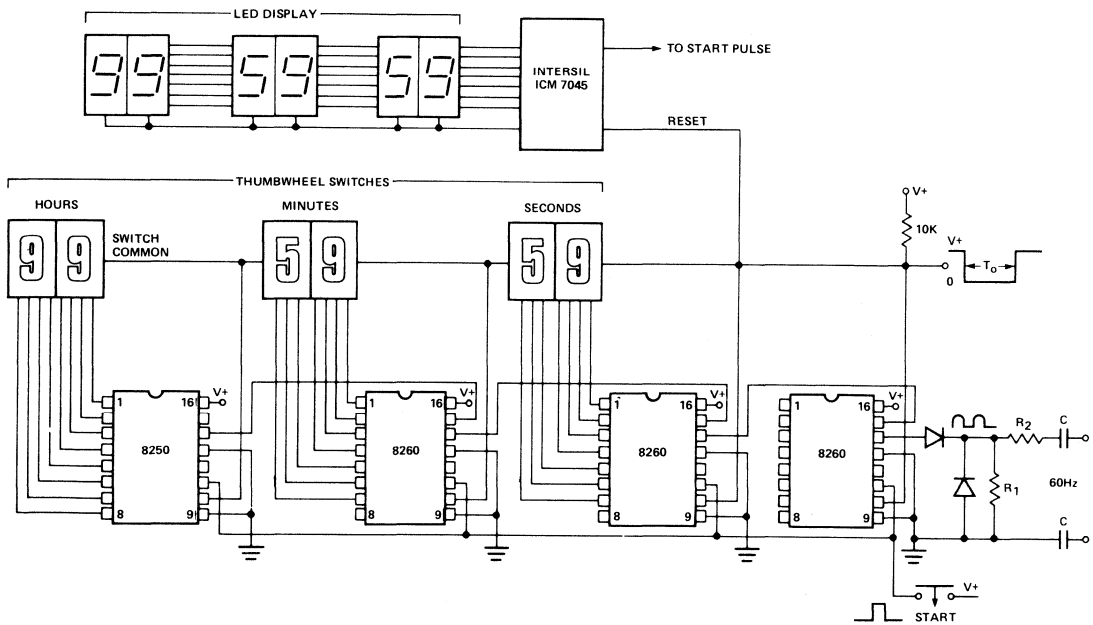


Figure 29. Programmable 100 Hour Timer with Display

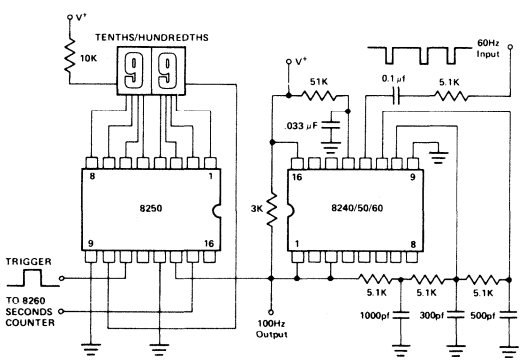


Figure 30. Front End for High Resolution Timer

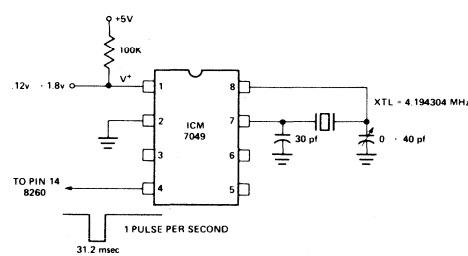


Figure 31. Intersil 7049 CMOS 1 Second Reference Oscillator

STAIRCASE GENERATOR

The open collector outputs of the 8240/50/60 counter stages are useful in several applications where digitally sequenced switches are needed. One example is the staircase generator of Figure 32. In this circuit an array of resistors is switched to ground to generate binary (or BCD) weighted currents. The op amp converts these currents to an output voltage. Under reset condition the switches are off and the output is at ground. When a trigger is applied the output goes to V_{REF} and generates a negative going staircase of 256 (or 100) levels. The time duration of each stop is equal to the time base period (T=RC). The amplitude of the staircase can be varied by changing the input reference voltage. The staircase can be stopped at any desired level by applying a "disable" signal to pin 14 as shown.

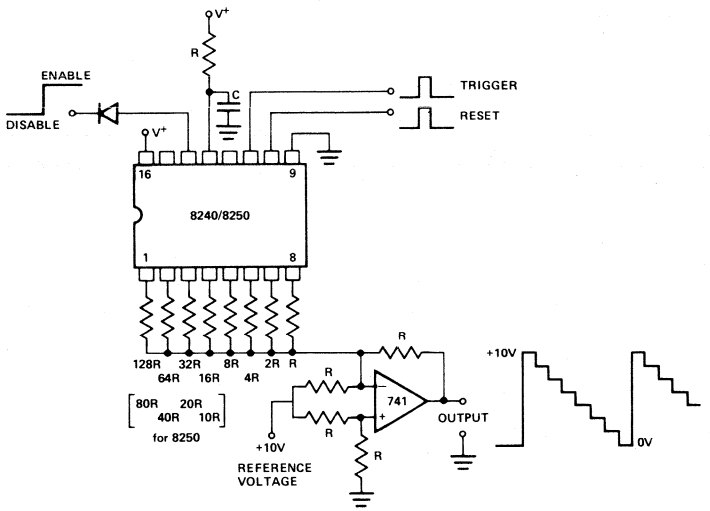


Figure 32. Staircase Generator

DIGITAL SAMPLE AND HOLD

By adding a comparator and RS flip flop to the staircase circuit we obtain the digital sample and hold shown in Figure 33. When a "strobe" input is applied, the 8240/8250 is first reset and then triggered through the small RC at pin 11 which delays the strobe signal. The strobe also sets the flip flop which in turn enables the counter via pin 14. The op amp goes to the high state and begins to count down at a rate set by the counter time base. When the op amp output reaches the analog input to be sampled, the comparator switches, resetting the flip flop and stops the count. The op amp output will accurately hold the sampled value until the next strobe pulse is applied. If the 8240/50 time base is set as shown, the maximum acquisition time would be 256 (or 100) times .01 msec, or approximately 2.6 msec.

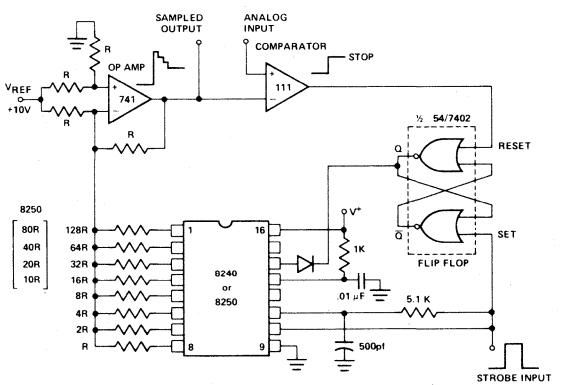


Figure 33. Digital Sample and Hold

ANALOG TO DIGITAL CONVERTER

Figure 34 shows an 8 bit binary (8240) or 2 digit BCD (8250) A/D converter using the staircase scheme of Figure 32. The operation is similar to the digital sample and hold of Figure 33 except digital outputs are taken off the counter output taps. In this circuit an input strobe pulse first resets then triggers the 8240/50 and sets the flip flop which enables the counter. The staircase from the op amp counts down until it reaches the analog input, at which time the comparator resets the flip flop and stops the count. The digital word at the 8 outputs is the complementary binary (or BCD) equivalent of the analog input. The maximum conversion time is again approximately 2.6 msec. The $\overline{Q}$ flip flop output is convenient to use as a data ready flag since its output goes high when the conversion is complete.

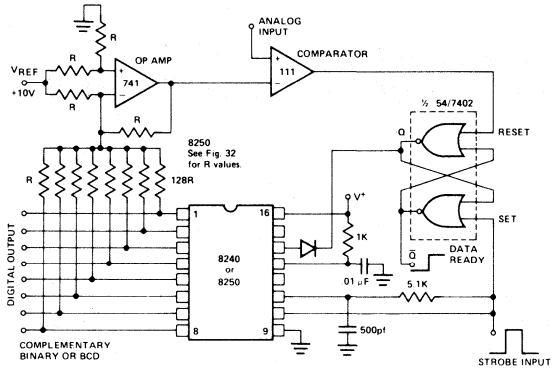


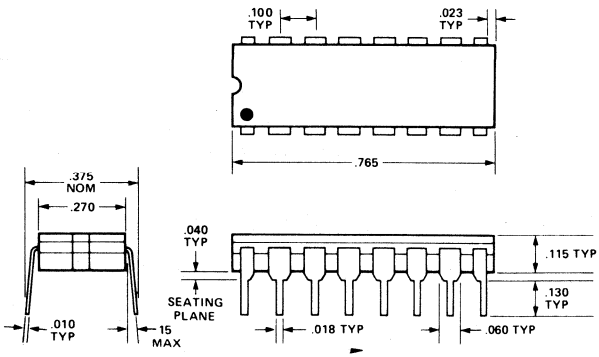
Figure 34. Analog-To-Digital Converter

ORDERING INFORMATION

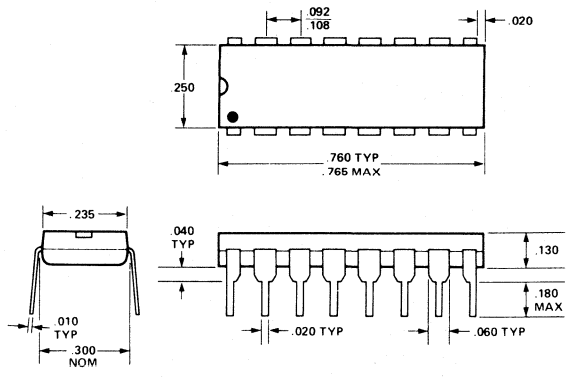
TYPE	MAXIMUM COUNT	TEMPERATURE RANGE	16 PIN PACKAGE	ORDER PART NUMBER
8240C	255	0°C to +75°C	Plastic DIP	ICL 8240 C PE
8240M	255	−55°C to +125°C	Ceramic DIP	ICL 8240 M DE
8250C	99	0°C to +75°C	Plastic DIP	ICL 8250 C PE
8250M	99	−55°C to +125°C	Ceramic DIP	ICL 8250 M DE
8260C	59	0°C to +75°C	Plastic DIP	ICL 8260 C PE
8260M	59	−55°C to +125°C	Ceramic DIP	ICL 8260 M DE

PACKAGE INFORMATION

16 PIN CERAMIC DIP (DE)



16 PIN PLASTIC DIP (PE)



D129 4-CHANNEL MOS FET SWITCH DRIVER WITH DECODE

D129

FEATURES

- Quad Three-Input Gates Decode Binary Counter to Four Lines
- Inputs Compatible with Low Power TTL and DTL, I_F = 200μA Max
- Output Current Sinking Capability 10mA
- External Pull-Up Elements Required
- Compatible with G115 and G123 Series Multichannel MOS FET Switches which include Current-Limiter Pull-Up FETs

ORDERING INFORMATION

D 129 M DD

- DD — Package: FD 14 pin flat (¼" x ¼") / DD 14 pin DIL Ceramic
- M — Temperature Range: M = -55°C to +125°C / I = -20°C to + 85°C
- 129 — Device Chip Type
- D — Analog Switch Driver

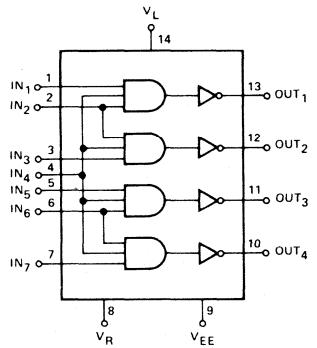
GENERAL DESCRIPTION

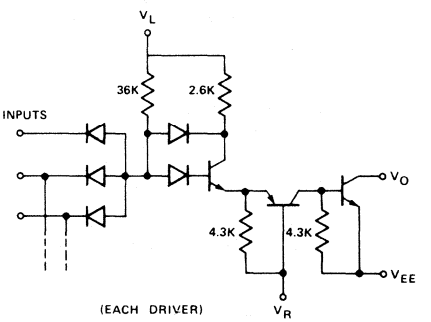
The D129 is a 4-channel driver with binary decode input. It has been designed to provide the DC level-shifting required to interface low-level logic outputs (0.7 to 2.2V) to field-effect transistor inputs (up to 50V peak-to-peak). For a 5V input logic supply, the V_{EE} terminal can be set at any voltage between -5V and -30V. The output transistor is capable of sinking 10mA and will stand-off up to 50V above V_{EE} in the off-state.

The ON state of the driver is controlled by a logic "1" (open) on all three input logic lines, while the OFF state of the driver is achieved by pulling any one of the three inputs to a logic "0" (ground).

The 4-channel driver is internally connected such that each one can be controlled independently or decoded from a binary counter.

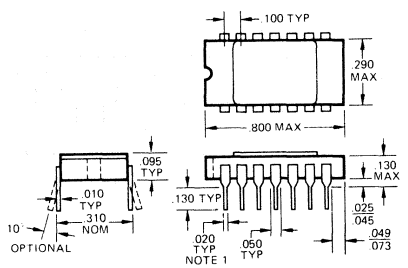
SCHEMATIC AND LOGIC DIAGRAMS



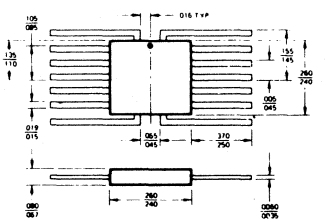


PACKAGE OUTLINES

14-PIN CERAMIC DUAL-IN-LINE PACKAGE



FLAT PACKAGE



ABSOLUTE MAXIMUM RATINGS

$V_O - V_{EE}$	50V
$V_R - V_{EE}$	33V
$V_L - V_R$	8V
$V_{IN} - V_R$	±6V
Current (any terminal)	30mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Power Dissipation (note)	750mW

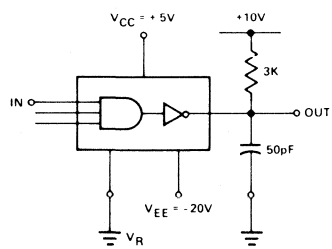
Note: Dissipation rating assumes device mounted with all leads welded or soldered to pc board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient termperatures.

ELECTRICAL CHARACTERISTICS Test conditions unless otherwise specified V_{EE} = -20V, V_R = 0V, V_L = 5V

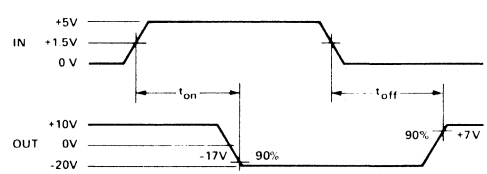
	PARAMETER		CONDITIONS		MAX LIMITS D129M -55°C	D129M 25°C	D129M 125°C	D129I -20°C	D129I 25°C	D129I 85°C	UNIT
OUT	V_{OL}	Output Voltage, Low	I_O = 10mA	V_{IN} = 2.2V, V_L = 4.5V	-19.3	-19.3	-19	-19.25	-19.25	-19	V
OUT	V_{OL}	Output Voltage, Low	I_O = 1mA	V_{IN} = 2.2V, V_L = 4.5V	-19.8	-19.8	-19.75				V
OUT	I_{OH}	Output Current, High	V_O= 10V, V_{IN} = 0.7V		0.1	0.1	20	0.2	0.2	10	µA
IN	I_{INH}*	Input Current Input Voltage High	V_{IN}= 5V Input Under Test, V_{IN}= 0 All Other Inputs		0.25	0.25	5	1	1	5	µA
IN	I_{INL}*	Input Current, Input Voltage Low	V_{IN}= 0, V_L= 5.5V		-250	-200	-160	-250	-225	-200	µA
TIME	t_{on}	Turn-ON Time	See Switching Time Test Circuit			0.25			0.3		µs
TIME	t_{off}	Turn-OFF Time	See Switching Time Test Circuit			1.0			1.5		µs
SUPPLY	I_{EE}	Negative Supply Current	V_{EE}= -20V, V_L= 5.5V	One Channel "ON"		- 2			- 2.25		mA
SUPPLY	I_L	Logic Supply Current	V_{EE}= -20V, V_L= 5.5V	One Channel "ON"		3			3.3		mA
SUPPLY	I_{EE}	Negative Supply Current	V_{EE}= -20V, V_L= 5.5V	All V_{IN} = 0, All Channels "OFF"		-10			-25		µA
SUPPLY	I_L	Logic Supply Current	V_{EE}= -20V, V_L= 5.5V	All V_{IN} = 0, All Channels "OFF"		0.75			1		mA

* Per gate Input

SWITCHING TIME AND TEST CIRCUIT



t_f = 100ns
t_r = 100ns
t_{pw} = 1µs
f = 100K Hz



HIGH-SPEED DRIVER WITH JUNCTION FET SWITCHES

DG 180, 181, 182, DG 183, 184, 185, DG 186, 187, 188, DG 189, 190, 191

FEATURES

- Constant ON-resistance with signals to ±10V with 75Ω max, ±7.5V with 10Ω max
- ±15V power supplies
- < 2nA leakage from signal channel in both ON and OFF states
- TTL, DTL, RTL direct drive compatibility
- t_{on}, t_{off} < 150ns, break-before-make action
- Cross-talk and open switch isolation, > 50dB at 10 MHz (75Ω load)

FUNCTIONAL DESCRIPTION

PART NUMBER	TYPE	R_{ON} (MAX)
DG 180	Dual SPST	10
DG 181	Dual SPST	30
DG 182	Dual SPST	75
DG 183	Dual DPST	10
DG 184	Dual DPST	30
DG 185	Dual DPST	75
DG 186	SPDT	10
DG 187	SPDT	30
DG 188	SPDT	75
DG 189	Dual SPDT	10
DG 190	Dual SPDT	30
DG 191	Dual SPDT	75

GENERAL DESCRIPTION

The DG180 thru DG191 series of analog gates consists of 2 or 4 N-channel junction-type field-effect transistors (J-FET) designed to function as electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2V) to control the ON-OFF state of each switch. The driver is designed to provide a turn-off speed which is faster than turn-on speed, so that break-before-make action is achieved when switching from one channel to another. In the ON state each switch conducts current equally well in either direction. In the OFF condition the switches will block voltages up to 20V peak-to-peak. Switch-OFF input-output feedthrough is > 50dB at 10MHz, because of the low output impedance of the FET-gate driving circuit.

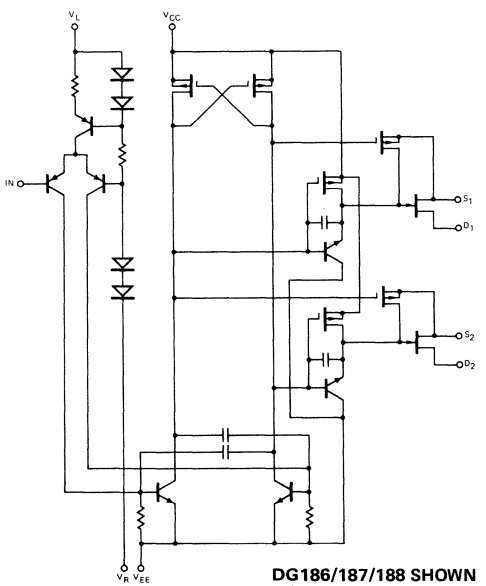
ANALOG GATE PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.

Precap Visual – Method 2010, Condition B.
Stabilization Bake – Method 1008.
Temperature Cycle – Method 1010.
Centrifuge – Method 2001, Condition E.
Hermeticity – Method 1014, Condition A,C.
(Leak Rate < 5×10^{-7} atm cc/s)

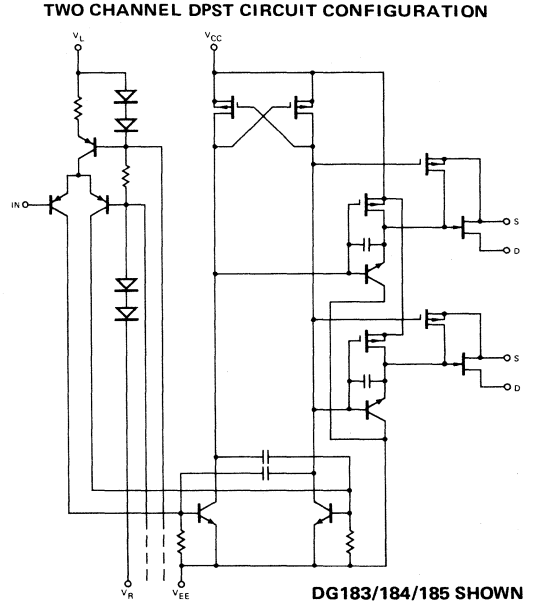
SCHEMATIC DIAGRAM (Typical Channel)

ONE AND TWO CHANNEL SPDT AND SPST CIRCUIT CONFIGURATION



DG186/187/188 SHOWN

TWO CHANNEL DPST CIRCUIT CONFIGURATION



DG183/184/185 SHOWN

MAXIMUM RATINGS

$V_{CC}-V_{EE}$	36V	V_L-V_{IN}	8V
$V_{CC}-V_D$	33V	V_L-V_R	8V
V_D-V_{EE}	33V	$V_{IN}-V_R$	8V
V_D-V_S	±22V	V_R-V_{EE}	27V
V_L-V_{EE}	36V	V_R-V_{IN}	2V
Current (Any Terminal except S or D)	See Note 3		30mA

Current (S or D) See Note 3	200 mA
Storage Temperature	–65°C to +150°C
Operating Temperature	–55°C to +125°C
Power Dissipation*	450 (TW), 750 (FLAT), 825 (DIP) mW

*Device mounted with all leads welded or soldered to PC board. Derate 6mW/°C (TW); 10mW/°C (FLAT); 11mW/°C (DIP) above 75°C.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15V, V_{EE} = –15V, V_L = 5V, V_R = 0, Unless Noted)

	PARAMETER	DEVICE	MAX LIMITS -55°C	+25°C	+125°C	-20°C	+25°C	+85°C	UNITS	TEST CONDITIONS (Note 1)
SWITCH	I_S (off)	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 10V, V_D = -10V, V_{CC} = 10V V_{EE} = -20V, V_{IN} = "off"
		DG181, 184, 187, 190 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 7.5V, V_D = -7.5V V_{IN} = "off"
		DG182, 185, 188, 191		1	100		5	100	nA	V_S = 10V, V_D = –10V V_{IN} = "off"
	I_D (off)	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 10V, V_D = -10V, V_{CC} = 10V V_{EE} = -20V, V_{IN} = "off"
		DG181, 184, 187, 190 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 7.5V, V_D = -7.5V V_{IN} = "off"
		DG182, 185, 188, 191		1	100		5	100	nA	V_S = 10V, V_D = -10V V_{IN} = "off"
	I_D (on) + I_S (on)	DG180, 181, 183, 184, 186, 187, 189, 190		-2	-200		-10	-200	nA	V_D = V_S = -7.5V, V_{IN} = "on"
		DG182, 183, 188, 191		-2	-200		-10	-200	nA	V_D = V_S = -10V, V_{IN} = "on"
IN	I_{INL}	ALL	-250	-250	-250	-250	-250	-250	µA	V_{IN} = 0V
	I_{INH}	ALL		10	20		10	20	µA	V_{IN} = 5V
DYNAMIC	t_{on}	10Ω Switches		300			350		ns	See switching time test circuit
		30Ω Switches		150			180			
		75Ω Switches		250			300			
	t_{off}	10Ω Switches		250			300			
		30Ω and 75Ω Switches		130			150			
	C_S (off)	DG181, 182, 184, 185, 187, 188, 190, 191 (DG180, 183, 186, 189)	9 typical (21 typical)						pF	V_S = -5V, I_D = 0, f = 1MHz
	C_D (off)		6 typical (17 typical)							V_D = +5V, I_S = 0, f = 1MHz
	$C_{D(on)}$ + $C_{S(on)}$		14 typical (17 typical)							V_D = V_S = 0, f = 1MHz
	Off Isolation		Typically > 50dB at 10MHz (See Note 2)							R_L = 75Ω, C_L = 3pF
SUPPLY	I_{CC}	DG180, 181, 182, 189 190, 191		1.5			1.5		mA	V_{IN} = "on"
		DG183, 184, 185		0.1			0.1			
		DG186, 187, 188		0.8			0.8			
	I_{EE}	DG180, 181, 182, 189 190, 191		-5.0			-5.0			
		DG183, 184, 185		-4.0			-4.0			
		DG186, 187, 188		-3.0			-3.0			
	I_L	DG180, 181, 182, 183 184, 185, 189, 190, 191		4.5			4.5			
		DG186, 187, 188		3.2			3.2			
	I_R	ALL		-2.0			-2.0			
	I_{CC}	DG180, 181, 182, 189, 190, 191		1.5			1.5			V_{IN} = "off"
		DG183, 184, 185		3.0			3.0			
		DG186, 187, 188		0.8			0.8			
	I_{EE}	DG180, 181, 182, 189, 190, 191		-5.0			-5.0			
		DG183, 184, 185		-5.5			-5.5			
		DG186, 187, 188		-3.0			-3.0			
	I_L	DG180, 181, 182, 183 184, 185, 189, 190, 191		4.5			4.5			
		DG186, 187, 188		3.2			3.2			
	I_R	ALL		-2.0			-2.0			

Note 1: See Switching State Diagrams for V_{IN} "ON" and V_{IN} "OFF" Test Conditons.
Note 2: Off Isolation typically >55dB at 1MHz for DG 180, 183, 186, 189.
Note 3: Saturation Drain Current for DG180, 183, 186, 189 only, typically 300mA (2msec Pulse Duration.) Maximum Current on all other devices (any terminal) 30mA.

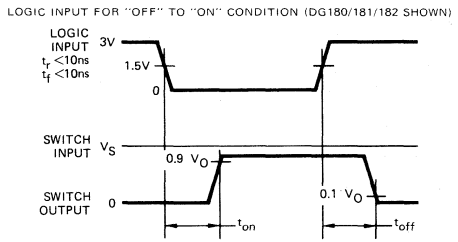
ELECTRICAL CHARACTERISTICS (CONT'D)
MAXIMUM ON RESISTANCES ($R_{DS(ON)}$ MAX)

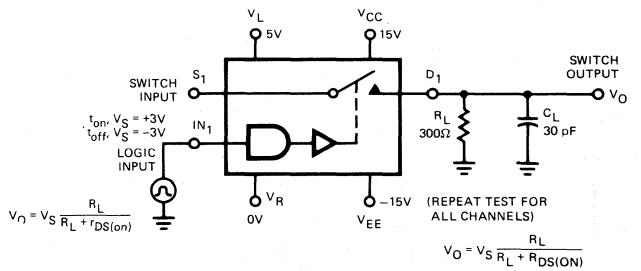
DEVICE NUMBER	MILITARY TEMPERATURE			INDUSTRIAL TEMPERATURE			UNITS	CONDITIONS (Note 1) V_{CC} = 15V, V_{EE} = -15V, V_L = 5V, V_R = 0V	
	-55°C	+25°C	+125°C	-20°C	+25°C	+85°C			
DG 180	10	10	20	15	15	25	Ω	V_D = -7.5V	
DG 181	30	30	60	50	50	75	Ω	V_D = -7.5V	
DG 182	75	75	100	100	100	150	Ω	V_D = -10V	
DG 183	10	10	20	15	15	25	Ω	V_D = -7.5V	
DG 184	30	30	60	50	50	75	Ω	V_D = -7.5V	
DG 185	75	75	150	100	100	150	Ω	V_D = -10V	I_S = -10 mA
DG 186	10	10	20	15	15	25	Ω	V_D = -7.5V	V_{IN} = "ON"
DG 187	30	30	60	50	50	75	Ω	V_D = -7.5V	
DG 188	75	75	150	100	100	150	Ω	V_D = -10V	
DG 189	10	10	20	15	15	25	Ω	V_D = -7.5V	
DG 190	30	30	60	50	50	50	Ω	V_D = -7.5V	
DG 191	75	75	150	100	100	150	Ω	V_D = -10V	

APPLICATION HINT (for design only): Normally the minimum signal handling capability of the DG180 through DG191 family is 20V peak-to-peak for the 75Ω switches and 15V peak-to-peak for the 10Ω and 30Ω switches (refer I_D and I_S tests above). For other Analog Signals, the following guidelines can be used: proper switch turn-off requires that $V_{EE} \leq V_{ANALOG}$ (-peak) -Vp ≤ 7.5V for the 10Ω and 30Ω switches and Vp ≤ 5.0V for 75Ω switches, i.e., A -10V minimum (-peak) analog signal and a 75Ω switch (Vp ≤ 5V), requires that $V_{EE} \leq$ -10V -5V = -15V.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





SWITCHING STATE DIAGRAMS

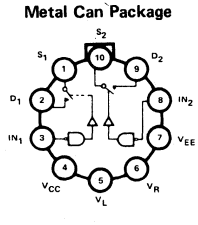
DUAL SPST
DG180/181/182

TEST CONDITIONS

DG180/181/182	
V_{IN} "ON" = 0.8V	All Channels
V_{IN} "OFF" = 2.0V	All Channels

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

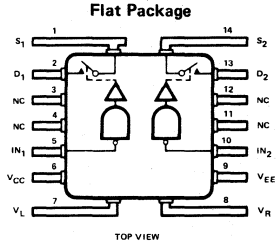
Metal Can Package



TOP VIEW

ORDER NUMBERS:
DG180AA OR DG180BA
DG181AA OR DG181BA
DG182AA OR DG182BA

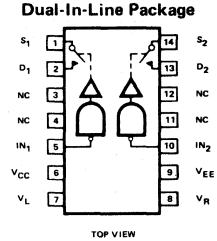
Flat Package



TOP VIEW

ORDER NUMBERS:
DG180AL OR DG180BL
DG181AL OR DG181BL
DG182AL OR DG182BL

Dual-In-Line Package



TOP VIEW

ORDER NUMBERS:
DG180AP OR DG181BP
DG181AP OR DG181BP
DG182AP OR DG182BP

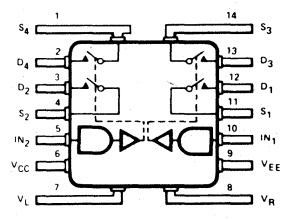
DUAL DPST
DG183/184/185

TEST CONDITIONS

DG183/184/185	
V_{IN} "ON" = 2.0V	All Channels
V_{IN} "OFF" = 0.8V	All Channels

SWITCH STATES ARE FOR LOGIC "0" INPUT = 0.8V

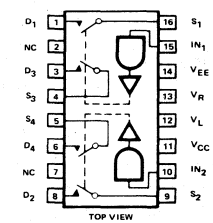
Flat Package



TOP VIEW

ORDER NUMBERS:
DG183AL OR DG183BL
DG184AL OR DG184BL
DG185AL OR DG185BL

Dual-In-Line Package



TOP VIEW

ORDER NUMBERS:
DL183AP OR DG183BP
DG184AP OR DG184BP
DG185AP OR DG185BP

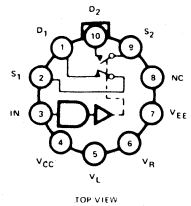
SPDT
DG186/187/188

TEST CONDITIONS

DG186/187/188	
V_{IN} "ON" = 2.0V	Channel 1
V_{IN} "ON" = 0.8V	Channel 2
V_{IN} "OFF" = 2.0V	Channel 2
V_{IN} "OFF" - 0.8V	Channel 1

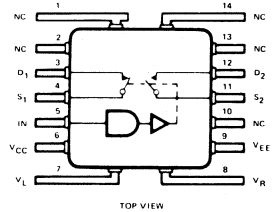
SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

Metal Can Package



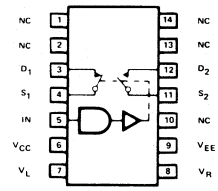
ORDER NUMBERS:
DG186AA OR DG186BA
DG187AA OR DG187BA
DG188AA OR DG188BA

Flat Package



ORDER NUMBERS:
DG186AL OR DG186BL
DG187AL OR DG187BL
DG188AL OR DG188BL

Dual-In-Line Package



ORDER NUMBERS:
DG186AP OR DG186BP
DG187AP OR DG187BP
DG188AP OR DG188BP

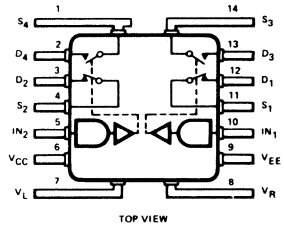
DUAL SPDT
DG189/190/191

TEST CONDITIONS

DG189/190/191	
V_{IN} "ON" = 2.0V	Channels 1 & 2
V_{IN} "ON" = 0.8V	Channels 3 & 4
V_{IN} "OFF" = 2.0V	Channels 3 & 4
V_{IN} "OFF" = 0.8V	Channels 1 & 2

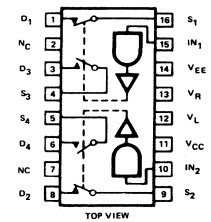
SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

Flat Package



ORDER NUMBERS:
DG189AL OR DG189BL
DG190AL OR DG190BL
DG191AL OR DG191BL

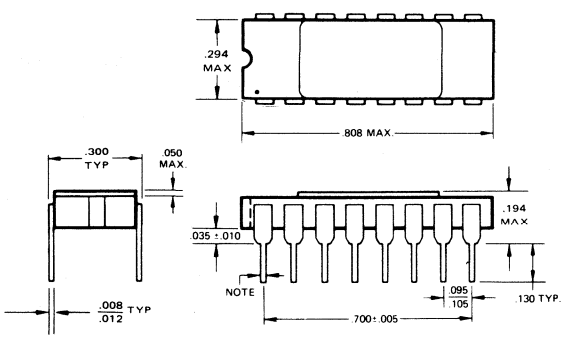
Dual-In-Line Package



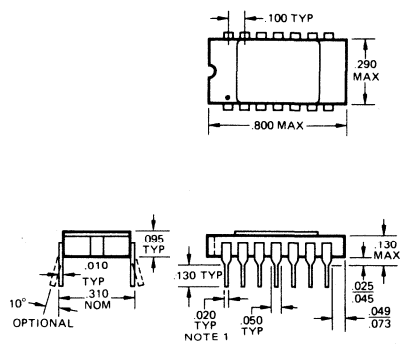
ORDER NUMBERS:
DG189AP OR DG189BP
DG190AP OR DG190BP
DG191AP OR DG191BP

PACKAGE DIMENSIONS

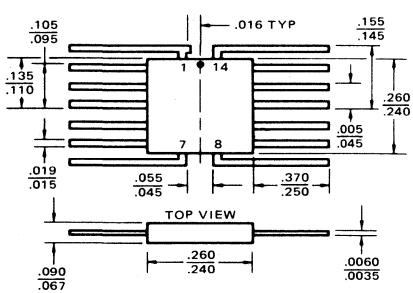
16 PIN CERAMIC PACKAGE



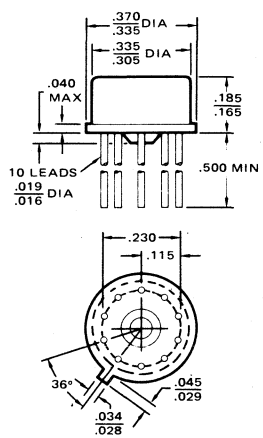
14 PIN CERAMIC PACKAGE



FLAT PACKAGE



TO-100 PACKAGE



NOTE: ALL DIMENSIONS IN INCHES.

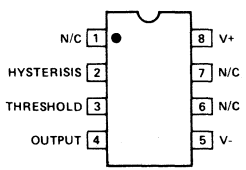
MICROPOWER VOLTAGE DETECTOR/ INDICATOR/VOLTAGE REGULATOR/ PROGRAMMABLE ZENER

ICL8211
ICL8212

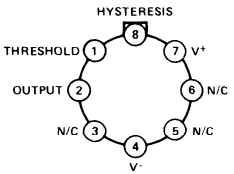
FEATURES

- High accuracy voltage sensing and generation: internal reference 1.15 volts typical
- Low sensitivity to supply voltage and temperature variations
- Wide supply voltage range: Typ. 1.8 to 30 volts
- Essentially constant supply current over full supply voltage range
- Easy to set hysteresis voltage range
- Defined output current limit - ICL8211
  High output current capability - ICL8212
- Innumerable useful applications including:
  1. Low voltage sensor/indicator
  2. High voltage sensor/indicator
  3. Non volatile out-of-voltage range sensor/indicator
  4. Programmable voltage reference or zener diode
  5. Series or shunt power supply regulator
  6. Fixed value constant current source

CONNECTION DIAGRAM



8 LEAD PLASTIC MINI DIP



TO99

Pin 1 is designated by either a dot or a notch for dual inline package.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL8211CPA	0 to +70°C	8 lead MiniDIP
ICL8211CTY	0 to +70°C	TO-99 Can
ICL8211MTY	-55 to +125°C	TO-99 Can
ICL8212CPA	0 to 70°C	8 lead MiniDIP
ICL8212CTY	0 to 70°C	TO-99 Can
ICL8212MTY	-55 to +125°C	TO-99 Can
ICL8211D	Dice only	
ICL8212D	Dice only	

GENERAL DESCRIPTION

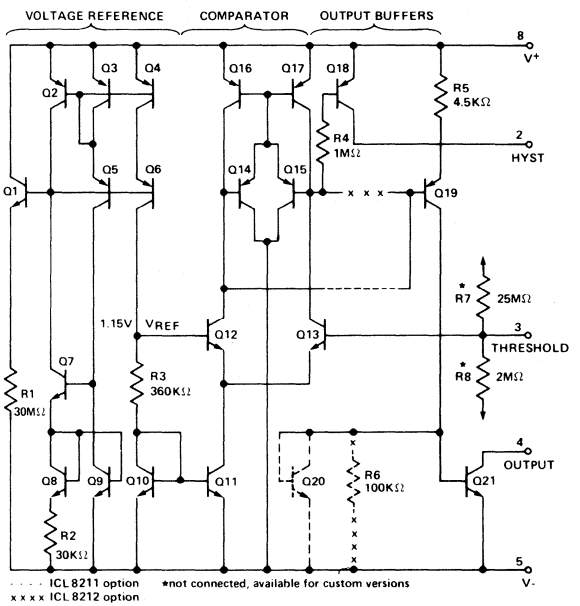
The Intersil ICL8211/12 are micropower bipolar monolithic integrated circuits intended primarily for precise voltage detection and generation. These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

Specifically, the ICL8211 provides a 7ma current limited output sink when the voltage applied to the 'THRESHOLD' terminal is less than 1.15 volts - the internal reference. The ICL8212 requires a voltage in excess of 1.15 volts to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS OUTPUT) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

Applications for the ICL8211/12 include a variety of voltage detection circuits such as low battery indicators (portable systems), power supply malfunction detectors for volatile memory systems, programmable zener diodes, both shunt and series power supply regulators, constant current sources.

The ICL8211/12 may be customized by the use of metal mask options to provide more complete integration on chip (including set resistors, etc.) for volume dedicated systems, thereby reducing component counts and cost.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage ($V^+ - V^-$)	-0.5 to +30 volts
Output Voltage (with respect to V^-)	-0.5 to + 30 volts
Hysteresis Voltage (with respect to V^+)	+0.5 to -10 volts
Threshold Input Voltage	+30 to -5 volts with respect to V^- and +0 to -30 volts with respect to V^+
Current into Any Terminal	±50mA
Power Dissipation (Note 2 & 3)	300mW
Operating Temperature Range ICL8211M/12M	-55°C to +125°C
Operating Temperature Range ICL8211C/12C	0 to +70°C
Storage Temperature Range	-55°C to +125°C

NOTE 1: Absolute maximum ratings define parameter limits that if exceeded may permanently damage or change the device.

NOTE 2: Rating applies for case temperatures to 125°C for ICL8211MTY/12MTY products. Derate linearly at -10mW/°C for ambient temperatures above 100°C.

NOTE 3: Derate linearly above 50°C by -10mW/°C for ICL8211C/12C products. The threshold input voltage may exceed +7 volts with respect to V- for short periods of time. However for continuous operation this voltage must be maintained at a value less than 7 volts.

TYPICAL OPERATING CHARACTERISTICS ($V^+ - V^- = 5V$, $T_A = 25°C$ unless otherwise specified)

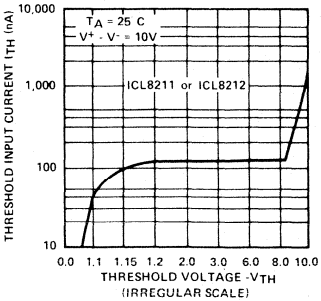
PARAMETER	SYMBOL	CONDITIONS	ICL8211			ICL8212			UNITS
			MIN	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Current	I^+	$2.0 < V^+ - V^- < 30$							
		$V_T = 1.3V$	10	22	40	50	110	250	µA
		$V_T = 0.9V$	50	140	250	10	20	40	µA
Threshold Trip Voltage	V_{TH}	I_{OUT} = 4mA $V^+ - V^-$ = 5V	0.98	1.15	1.19	1.00	1.15	1.19	V
		V_{OUT} = 2V $V^+ - V^-$ = 2V	0.98	1.145	1.19	1.00	1.145	1.19	V
		$V^+ - V^-$ = 30V	1.00	1.165	1.20	1.05	1.165	1.20	V
Threshold Voltage Disparity Between Output & Hysteresis Output	V_{THP}	I_{OUT} = 4mA V_{OUT} = 2V I_{HYST} = 7µA V_{HYST} = 3V		-8.0			-0.5		mV
Guaranteed Operating Supply Voltage Range	V_{OP}	+25°C	2.0		30	2.0		30	V
		0 to +70°C	2.2		30	2.2		30	V
		-55°C to +125°C	2.8		30	2.8		30	V
Typical Operating Supply Voltage Range	V_{OP}	+25°C	1.8		30	1.8		30	V
		+125°C	1.4		30	1.4		30	V
		-55°C	2.5		30	2.5		30	V
Threshold Voltage Temperature Coefficient	I_{VTH}	I_{OUT} = 4mA V_{OUT} = 2V		+200			+200		ppm/°C
Variation of Threshold Voltage with Supply Voltage	Δ_{VTH}	$\Delta(V^+ - V^-) = 10\%$ at $V^+ - V^- = 5V$		1.0			1.0		mV
Threshold Input Current	I_{TH}	V_{TH} = 1.15V		100	250		100	250	nA
		V_{TH} = 1.00V		5			5		nA
Output Leakage Current	I_{LO}	V_{OUT} = 30V V_{TH} = 1.0V						10	µA
		V_{OUT} = 30V V_{TH} = 1.3V			10				µA
		V_{OUT} = 5V V_{TH} = 1.0V						1	µA
		V_{OUT} = 5V V_{TH} = 1.3V			1				µA
Output Saturation Voltage	V_{SAT}	I_{OUT} = 4mA V_{TH} = 1.0V		0.17	0.4				V
		V_{TH} = 1.3V					0.17	0.4	V
Max Available Output Current	I_{HO}	(Note 4 & 5) V_{TH} = 1.0V	4	7.0	12				mA
		V_{OUT} = 5V V_{TH} = 1.3V				15	35		mA
		$-55°C \leq T_A \leq 125°C$ V_{TH} = 1.0V			15	12			mA
Hysteresis Leakage Current	I_{QHYST}	$V^+ + V^-$ = 10V V_{TH} = 1.0V $V_{HYST} = V^-$			0.1			0.1	µA
Hysteresis Sat Voltage	$V_{SATHYST}$	I_{HYST} = -7µA V_{TH} = 1.3V measured with respect to V^+		-0.1	-0.2		-0.1	-0.2	V
Max Available Hysteresis Current	I_{HHYST}	V_{TH} = 1.3V	-15	-21		-15	-21		µA

NOTE 4: The maximum output current of the ICL8211 is limited by design to 15ma under any operating condition. The output voltage may be sustained at any voltage up to +30 with respect to V^- as long as the maximum power dissipation of the device is not exceeded.

NOTE 5: The maximum output current of the ICL8212 is not defined and systems using the ICL8212 must therefore ensure that the output current does not exceed 50ma and that the maximum power dissipation of the device is not exceeded.

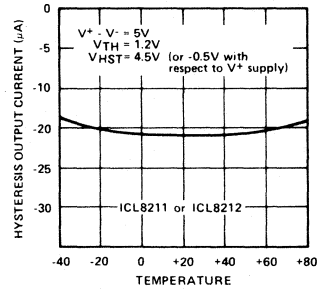
TYPICAL OPERATING CHARACTERISTICS

THRESHOLD INPUT CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



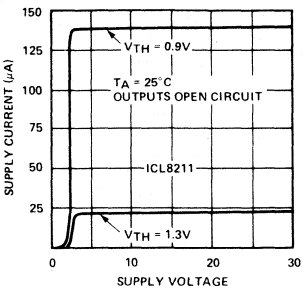
Characteristics common to both the ICL8211 and the ICL8212

HYSTERESIS OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE

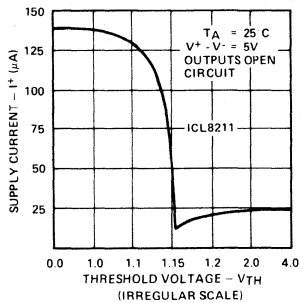


Characteristics ICL8211

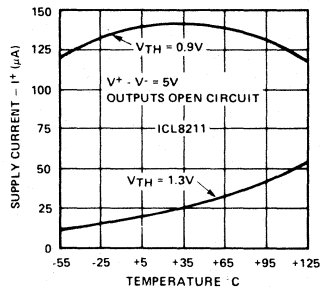
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



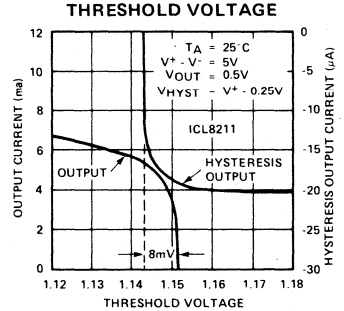
SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



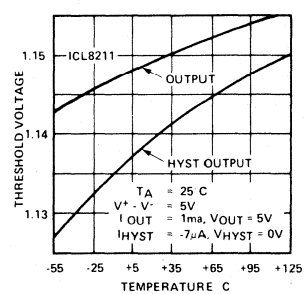
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



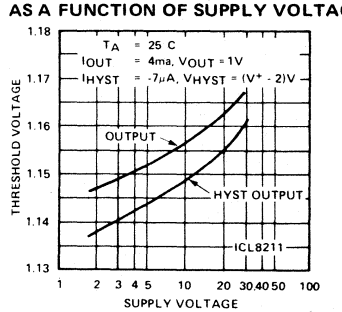
OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



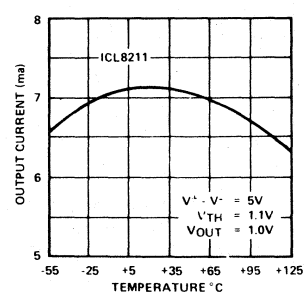
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



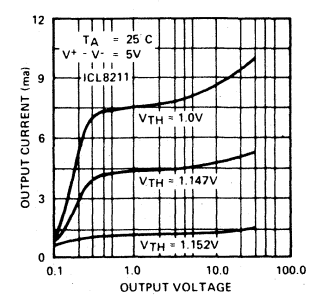
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE



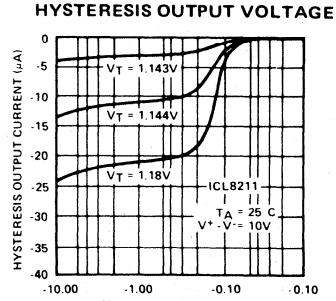
OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE



OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



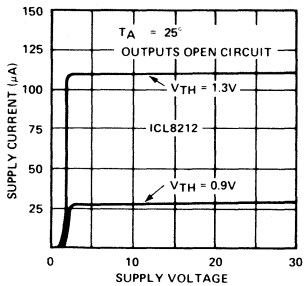
HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



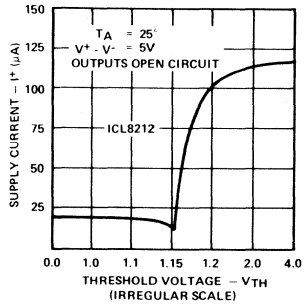
TYPICAL OPERATING CHARACTERISTICS

Characteristics ICL8212

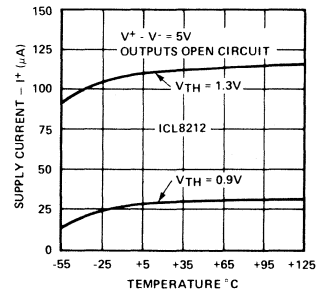
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



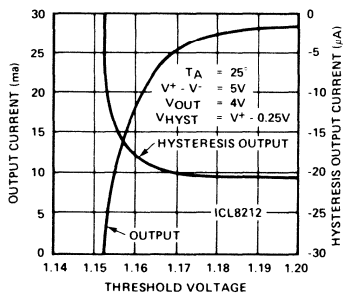
SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



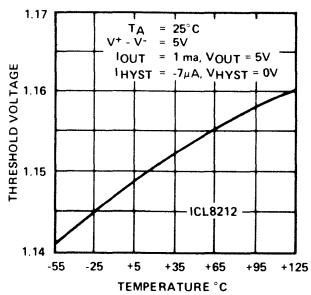
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



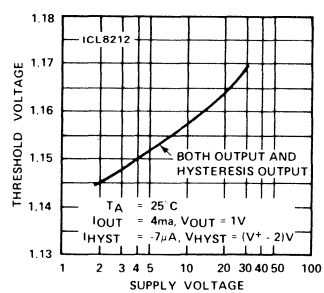
OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



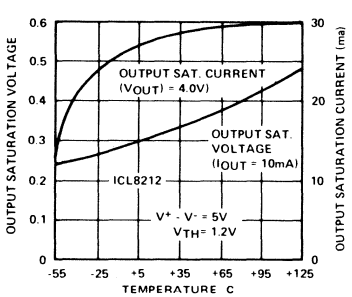
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



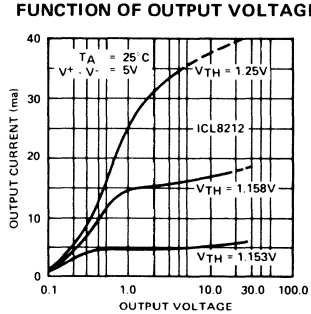
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE



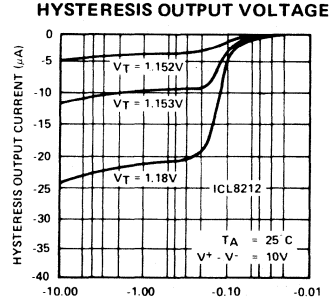
OUTPUT SATURATION VOLTAGE AND CURRENT AS A FUNCTION OF TEMPERATURE



OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



CIRCUIT DESCRIPTION

The ICL8211 and ICL8212 use a standard linear bipolar integrated circuit technology with high value thin film resistors. The reason for the use of thin film resistors is to be able to define extremely low value currents.

Components Q_1 thru Q_{10} and R_1, R_2 and R_3 set up an accurate voltage reference of 1.15 volts. This reference voltage is close to the value of the bandgap voltage for silicon and is highly stable with respect to both temperature and supply voltage. The deviation from the bandgap voltage is necessary due to the negative temperature coefficient of the thin film resistors (-5000 ppm per °C).

Components Q_2 thru Q_9 and R_2 make up a constant current source. Q_2 and Q_3 are identical and form a current mirror. Q_8 has 7 times the emitter area of Q_9. Due to the current mirror the collector currents of Q_8 and Q_9 are

forced to be equal and it can be shown that the collector current in Q_8 and Q_9 is

$$I_C\ (Q_8 \text{ or } Q_9) = \frac{1}{R_2} \times \frac{kT}{q} \ln 7$$

or approximately 1μA at 25°C

Where k = Boltzman's constant

q = charge on an electron

and T = absolute temperature in °K

Transistors Q_5, Q_6, and Q_7 assure that the collector to emitter voltage of Q_3, Q_4, and Q_9 remain constant with supply voltage variations thereby guaranteeing that the value of the constant current source is insensitive to supply voltage variations.

The base current of Q_1 provides sufficient current to ensure that the current source will start up; there being two stable states for this type of circuit - either as defined above or OFF if no start up current is provided. Leakage current in the transistors is not sufficient in itself to guarantee reliable startup.

Q_4 is matched to Q_3 and Q_2; and, Q_{10} is matched to Q_9. Thus the collector current and base emitter voltage Q_{10} are identical to that of Q_9 or Q_8. To generate the bandgap voltage it is necessary to sum a voltage equal to the base emitter voltage Q_9 to a voltage proportional to the difference of the base emitter voltages of two transistors Q_8 and Q_9 operating at two current densities.

$$\text{Thus } 1.15 = V_{BE}\ (Q_9 \text{ or } Q_{10}) + \frac{R_3}{R_2} \times \frac{kT}{q} \ln 7$$

$$\text{which provides } \frac{R_3}{R_2} = 12 \text{ (approx.)}$$

The total supply current consumed by the voltage reference section is approximately 6μA at room temperature. An input voltage at the THRESHOLD input is compared to the reference voltage 1.15 volts by the comparator consisting of transistors Q_{11} thru Q_{17}. The outputs from the comparator taken from the collectors of Q_{16} and Q_{17} are limited to two diode drops less than V^+ or approximately 1.1 volts. Thus the base current into the hysteresis output transistor is limited to about 500nA and the collector current of Q_{19} to 100μA.

In the case of the ICL8211, Q_{21} is proportioned to have 70 times the emitter area of Q_{20} thereby limiting the output current to approximately 7ma whereas, for the ICL8212 almost all the collector current of Q_{19} is available for base drive to Q_{21} resulting in a maximum available collector current of the order of 30ma.

APPLICATIONS

The ICL8211 and ICL8212 are similar in many respects especially with regard to the setup of the input trip conditions and hysteresis circuitry. The following discussion describes both devices and where differences occur they are clearly noted.

1. GENERAL INFORMATION

THRESHOLD INPUT CONSIDERATIONS

Any voltage may be applied to the THRESHOLD terminal having a value between -5 volts with respect to V^- to a maximum of V^+ as long as the absolute value of the peak to peak input does not exceed 30 volts. It is recommended however, that the THRESHOLD voltage does not exceed about +6 volts with respect to V^- since above that voltage the threshold input current increases sharply.

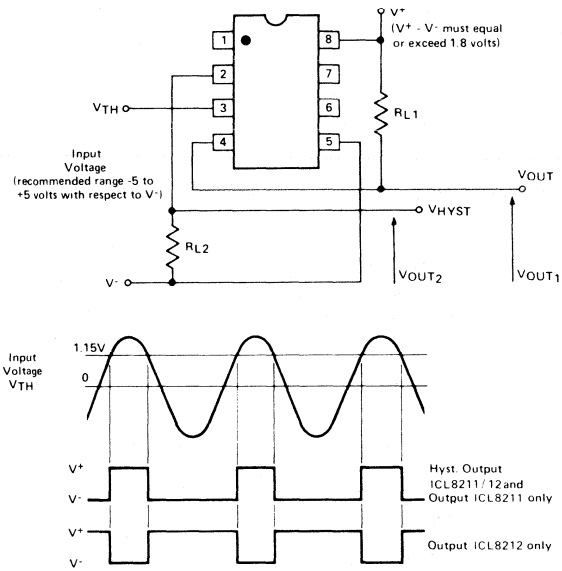


FIGURE 1 – VOLTAGE LEVEL DETECTION

The outputs change states with an input THRESHOLD voltage of approximately 1.15 volts. Input and output waveforms are shown in Figure 1 for a simple 1.15 volt level detector.

The HYSTERESIS output is a low current output and is intended primarily for input threshold voltage hysteresis applications. If this output is used for other applications it is suggested that output currents be limited to 10μA or less.

The regular OUTPUT's from either the ICL8211 or ICL-8212 may be used to drive most of the common logic families such as TTL or C-MOS using a single pullup resistor. The guaranteed TTL fanout for the ICL8211 is 2 and for the ICL8212 is 4.

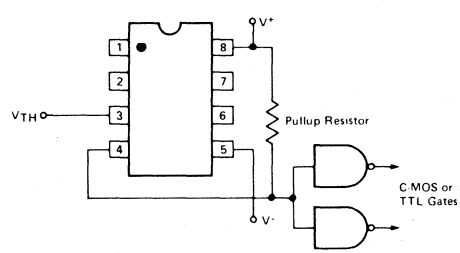


FIGURE 2 – OUTPUT LOGIC INTERFACE

A principal application of the ICL8211 is voltage level detection and for that reason the OUTPUT current has been limited to typically 7ma to permit direct drive to an LED lamp connected to the positive supply V^+ without a series current limiting resistor.

On the other hand the ICL8212 is intended for many applications such as programmable zener references and voltage regulators where output currents well in excess of 7ma are desirable. Therefore, the output of the ICL8212 is not current limited. If however, the output is used to drive an LED lamp then a series current limiting resistor must be used.

In many applications an input resistor divider network will be used. It is recommended that the current in this resistor network necessary to produce 1.15 volts be as follows. If the current in this network is of no concern, a current of 50μA may be used. If the current is a concern (battery operated systems) it is suggested a current of 6 to 8 μA represents a good compromise between accuracy and low power. Lower currents than 6μA are usable if accuracy is not important. The inaccuracy at lower currents is due to the input current of the device becoming a significant percentage of the current flowing in the resistor network.

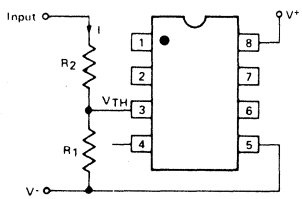


FIGURE 3 – INPUT RESISTOR NETWORK CONSIDERATIONS

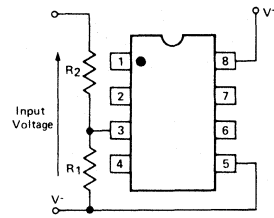
Case 1. High accuracy required, current in resistor network unimportant Set I = 50μA for V_{TH} = 1.15 volts $\therefore R_1 \Rightarrow$ 20K ohms.

Case 2. Good accuracy required, current in resistor network important Set I = 7.5μA for V_{TH} = 1.15 volts $\therefore R_1 \Rightarrow$ 150 K ohms.

SETUP PROCEDURES FOR VOLTAGE LEVEL DETECTION

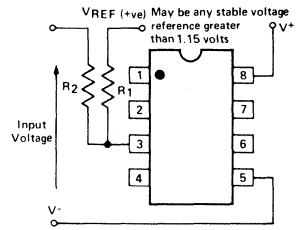
Case 1. Simple voltage detection - no hysteresis

Unless an input voltage of approximately 1.15 volts is to be detected, resistor networks will be used to divide or multiply the unknown voltage to be sensed. Figure 4 shows procedures on how to set up resistor networks to detect INPUT VOLTAGES of any magnitude and polarity with respect to the negative supply V^-.



a) Range of input voltage greater than +1.15 volts with respect to V^-.
Input voltage to change the output states

$$= \frac{(R_1 + R_2)}{R_1} \times 1.15 \text{ volts}$$



b) Range of input voltage less than +1.15 volts with respect to V^-.
Input voltage to change the output states

$$= \frac{(R_1 + R_2) \times 1.15}{R_1} - \frac{R_2 \, V_{REF}}{R_1}$$

FIGURE 4 – INPUT RESISTOR NETWORK SETUP PROCEDURES

For supply voltage level detection applications the input resistor network is connected across the supply terminals as shown in Figure 5.

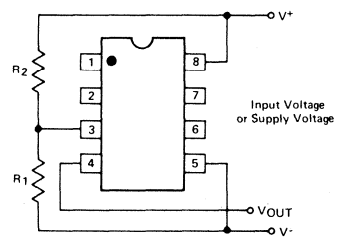


FIGURE 5 – COMBINED INPUT AND SUPPLY VOLTAGES

Conditions for correct operation of OUTPUT (terminal #4).

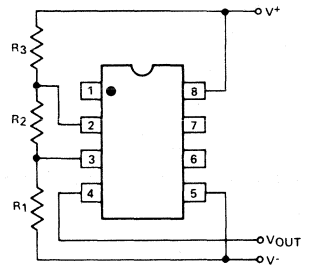
1. ICL8211
   1.8 volts $\leqslant$ Supply Voltage $\leqslant$ 30 volts
2. ICL8212
   0 $\leqslant$ Supply Voltage $\leqslant$ 30 volts

Case 2. Use of the HYSTERESIS function

The disadvantage of the simple detection circuits is that there is a small but finite input range whereby the outputs are neither totally 'ON' nor totally 'OFF'. The principle behind hysteresis is to provide positive feedback to the input trip point such that there is a voltage difference between the input voltage necessary to turn the outputs ON and to turn the outputs OFF.

The advantage of hysteresis is especially apparent in electrically noisy environments where simple but positive voltage detection is required. Hysteresis circuitry, however, is not limited to applications requiring better noise performance but may be expanded into highly complex systems with multiple voltage level detection and memory applications – refer to specific applications section.

There are two simple methods to apply hysteresis to a circuit for use in supply voltage level detection. These are shown in Figure 6.

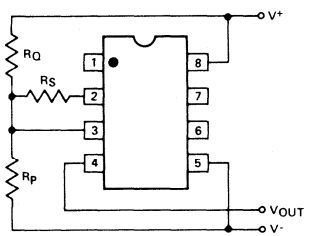


a) Low trip voltage

$$V_{TR1} = \left[\frac{(R_1 + R_2) \times 1.15}{R_1} + 0.1\right] \text{ volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_1 + R_2 + R_3)}{R_1} \times 1.15 \text{ volts}$$



b) Low trip voltage

$$V_{TR1} = \left[\frac{R_Q R_S}{(R_Q + R_S)} + R_P\right] \times \frac{1}{R_P} \times 1.15 \text{ volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_P + R_Q)}{R_P} \times 1.15 \text{ volts}$$

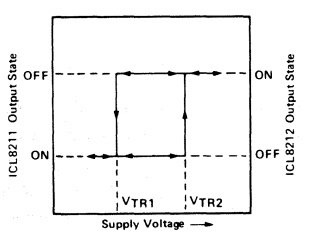


FIGURE 6 – Two alternative voltage detection circuits employing hysteresis to provide pairs of well defined trip voltages.

Circuit (a) requires that the full current flowing in the resistor network be sourced by the HYSTERESIS output whereas for circuit (b) the current to be sourced by the HYSTERESIS output will be a function of the ratio of the two trip points and their values. For low values of hysteresis circuit (b) is to be preferred due to the offset voltage of the hysteresis output transistor.

A third way to obtain hysteresis (ICL8211 only) is to connect a resistor between the OUTPUT and the THRESHOLD terminals thereby reducing the total external resistance connected between the THRESHOLD and V⁻ terminals when the OUTPUT is switched on.

3. PRACTICAL APPLICATIONS

a) Low Voltage Battery Indicator

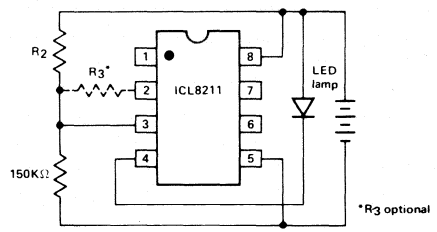


FIGURE 7 – LOW VOLTAGE BATTERY INDICATOR

This application is particularly suitable for portable or remote operated equipment which requires an indication of a depleted or discharged battery. The quiescent current taken by the system will be typically 35μA which will increase to 7ma when the lamp is turned on. R_3 will provide hysteresis if required.

b) |Non-Volatile| Low Voltage Detector

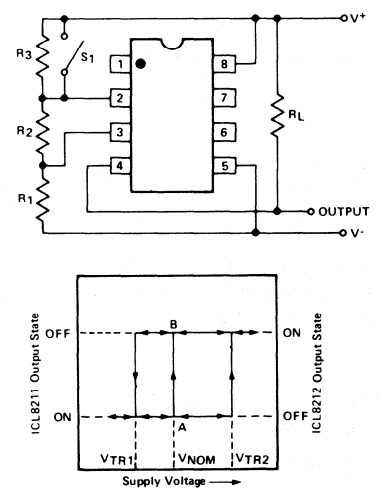


FIGURE 8 – LOW VOLTAGE DETECTOR AND MEMORY

In this application the high trip voltage V_{TR2} is set to be above the normal supply voltage range. On power up the initial condition is A. On momentarily closing switch S_1 the operating point changes to B and will remain at B until the

supply voltage drops below V_{TR1} when the output will revert to condition A. Note that state A is always retained if the supply voltage is reduced below V_{TR1} (even to zero volts) and then raised back to V_{NOM}.

c) (Non-volatile) Power Supply Malfunction Recorder

In many systems a transient or an extended abnormal (or absence of a) supply voltage will cause a system failure. This failure may take the form of information lost in a volatile semiconductor memory stack, a loss of time in a timer or even possible irreversible damage to components if a supply voltage exceeds a certain value.

There is, therefore, a need to be able to detect and store a record that an **out-of-operating range** supply voltage condition has occurred, even in the case where a supply voltage may have dropped to zero. On power up to the normal operating voltage the record must have been retained and easily interrogated. This could be important in the case of, say, a transient power failure due to a faulty component or intermittent power supply, open circuit, etc., where direct observation of the failure is difficult.

A simple circuit to record an out of range voltage excursion may be constructed using an ICL8211, an ICL8212 plus a few resistors. This circuit will operate to 30 volts without exceeding the maximum ratings of the I.C.'s. The two voltage limits defining the in range supply voltage may be set to any value between 2.0 and 30 volts.

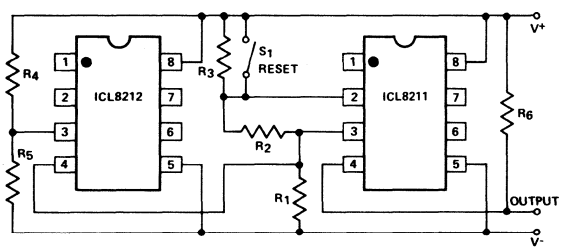


FIGURE 9 – SCHEMATIC OF RECORDER

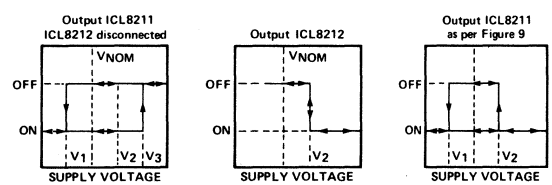


FIGURE 10 – OUTPUT STATES OF THE ICL8211 AND ICL8212 AS A FUNCTION OF THE SUPPLY VOLTAGE

Referring to Figure 9, the ICL8212 is used to detect a voltage V_2 which is the upper voltage limit to the operating voltage range. The ICL8211 detects the lower voltage limit of the operating voltage range V_1. Hysteresis is used with the ICL8211 so that the output can be stable in either state over the operating voltage range V_1 to V_2 by making V_3 - the upper trip point of the ICL8211 much higher in voltage than V_2.

The output of the ICL8212 is used to force the output of the ICL8211 into the ON state above V_2. Thus there is no value of the supply voltage that will result in the output of the ICL8211 changing from the ON state to the OFF state. This may be achieved only by shorting out R_3 for values of supply voltage between V_1 and V_2.

d) Constant Current Sources

The ICL8212 may be used as a constant current source of value of approximately 25μA by connecting the THRESHOLD terminal to the V⁻ terminal. Similarly the ICL8211 will provide a 130μA constant current source. The equivalent parallel resistance is in the tens of megohms over the supply voltage range of 2 to 30 volts. These constant current sources may be used to provide biasing for various circuitry including differential amplifiers and comparators. See Typical Operating Characteristics for complete information.

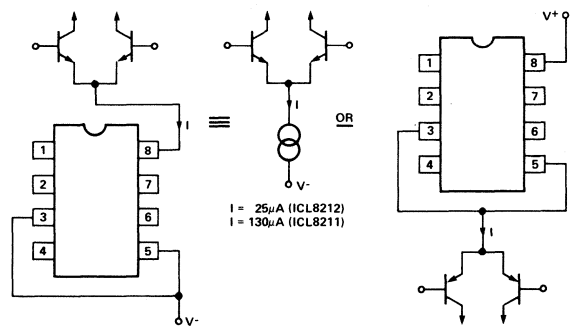


FIGURE 11 – CONSTANT CURRENT SOURCE APPLICATIONS

e) Zener or Precision Voltage Reference

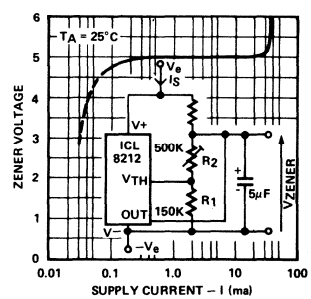


FIGURE 12 – PROGRAMMABLE ZENER OR VOLTAGE REFERENCE

The ICL8212 may be used to simulate a zener diode by connecting the OUTPUT terminal to the V_Z output and using a resistor network connected to the THRESHOLD terminal to program the zener voltage ($V_{ZENER} = \frac{(R_1 + R_2)}{R_1} \times 1.15$ volts).

Since there is no internal compensation in the ICL8212 it is necessary to use a large capacitor across the output to prevent oscillation.

Zener voltages from 2 to 30 volts may be programmed and typical impedance values between 300μA and 25ma will range from 4 to 7 ohms. The knee is sharper and occurs at a significantly lower current than other similar devices available.

f) Precision Voltage Regulators

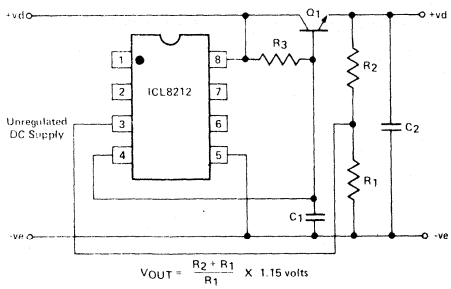


FIGURE 13 – SIMPLE VOLTAGE REGULATOR

The ICL8212 may be used as the controller for a highly stable series voltage regulator. The output voltage is simply programmed using a resistor divider network R_1 and R_2. Two capacitors C_1 and C_2 are required to ensure stability since the ICL8212 is uncompensated internally.

This regulator may be used with lower input voltages than most other commercially available regulators and also consumes less power for a given output control current than any commercial regulator. Applications would therefore include battery operated equipment especially those operating at low voltages.

f) High supply voltage dump circuit

In many circuit applications it is desirable to remove the power supply in the case of high voltage overload. For circuits consuming less than 5ma this may be achieved using an ICL8211 driving the load directly. For higher load currents it is necessary to use an external pnp transistor or darlington pair driven by the output of the ICL8211. Resistors R_1 and R_2 set up the disconnect voltage and R_3 provides optional voltage hysteresis if so desired.

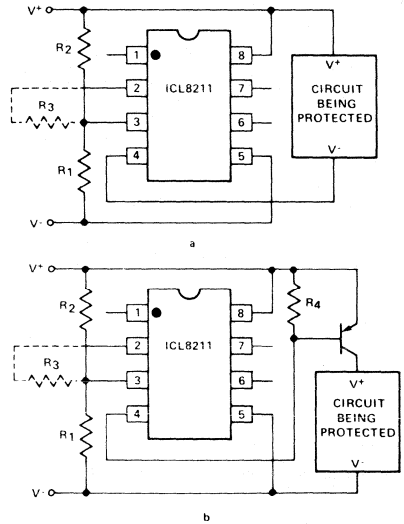


FIGURE 14 – HIGH VOLTAGE DUMP CIRCUITS

g) Frequency limit detectors

Simply frequency limit detectors providing a go/no-go output for use with varying amplitude input signals may be conveniently implemented with the ICL8211/12 devices. In the application shown the first device ICL8212 is used as a zero crossing detector. The output circuit consisting of R_3, R_4 and C_2 results in a slow output positive ramp. The negative range is much faster than the positive range. R_5 and R_6 provide hysteresis so that under all circumstances the second ICL8212 is turned on for sufficient time to discharge C_3 to V⁻. The time constant of R_7 C_3 is much greater than R_4 C_2. Depending upon the desired output polarities for low and high input frequencies either an ICL8211 or an ICL8212 may be used as the output driver.

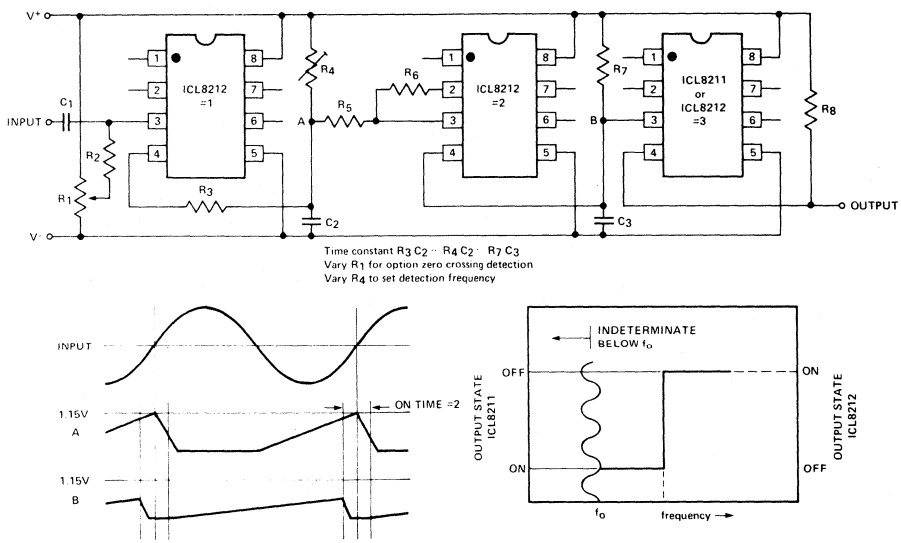


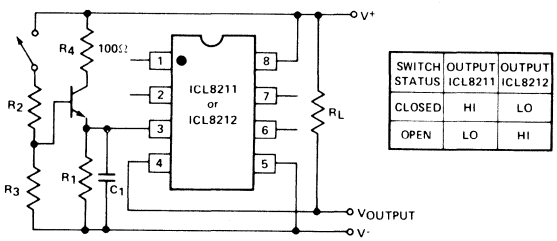
FIGURE 15 – FREQUENCY LIMIT DETECTOR

This circuit is sensitive to supply voltage variations and should be used with a stabilized power supply. At very low frequencies the output will switch at the input frequency.

h) Switch bounce filter

Single pole single throw (SPST) switches are less costly and more available than single pole double throw (SPDT) switches. SPST switches range from push button types, slide types to calculator keyboard types. A major problem with the use of SPST switches is the mechanical bounce of the electrical contacts on closure. Contact bounce times can range from a fraction of a millisecond to several tens of milliseconds depending upon the switch type. During this contact bounce time the switch may make and break contact several times.

The circuit shown in Figure 16 provides a rapid charge up of C_1 to close to the positive supply voltage (V^+) on a switch closure and a corresponding slow discharge of C_1 on a switch break. By proportioning the time constant of R_1 C_1 to approximately the manufacturer's bounce time the output at terminal #4 of the ICL8211/12 will be a single transition of state per desired switch closure.



SWITCH STATUS	OUTPUT ICL8211	OUTPUT ICL8212
CLOSED	HI	LO
OPEN	LO	HI

FIGURE 16 – SWITCH BOUNCE FILTER

j) Low voltage power disconnector

There are some classes of circuits that require the power supply to be disconnected if the power supply voltage falls below a certain value. As an example, the National LM199 precision reference has an on chip heater which malfunctions with supply voltages below 9 volts causing an excessive device temperature. The ICL8212 may be used to detect a power supply voltage of 9 volts and turn the power supply off to the LM199 heater section below that voltage.

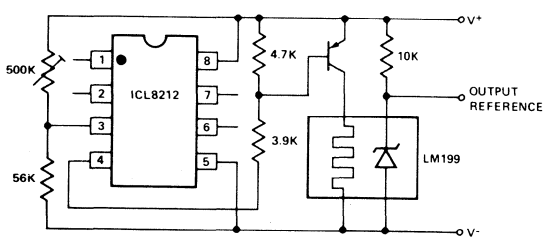


FIGURE 17 – LOW VOLTAGE POWER SUPPLY DISCONNECT

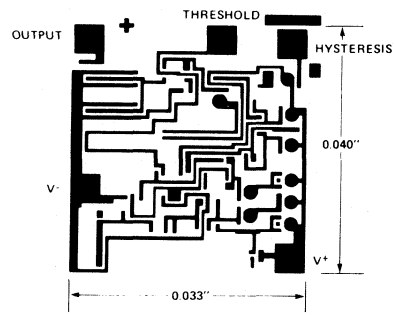
CUSTOM OPTIONS

The ICL8211/12 have been designed with more on chip components than are used, in anticipation of more dedicated high volume system usage. The trigger voltage and hysteresis resistor network is integrated on chip but not connected. Consult the factory for more information on custom options.

DICE INFORMATION

ICL8211/12 dice may be die bonded using either eutectic or epoxy techniques, and may either be thermocompression gold ball or ultrasonic wire bonded.

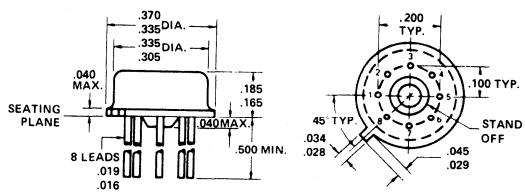
CHIP TOPOGRAPHY



Die is passivated with a deposited oxide. Bonding pad oxide windows are 3.6 x 3.6 mils square.

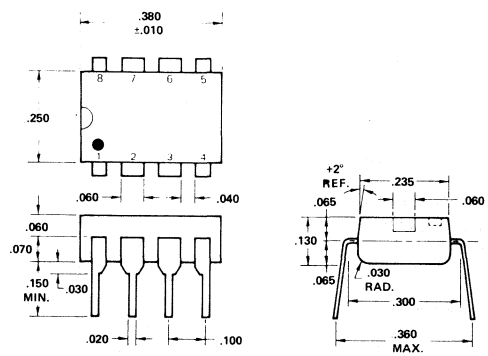
PACKAGE DIMENSIONS

TO-99



NOTES: All dimensions in inches
Leads are gold-plated Kovar

8 LEAD PLASTIC DIP



NOTE: Board drilling dimensions will equal standard practices for .020 diameter lead.

CMOS ANALOG GATE

IH200

FEATURES

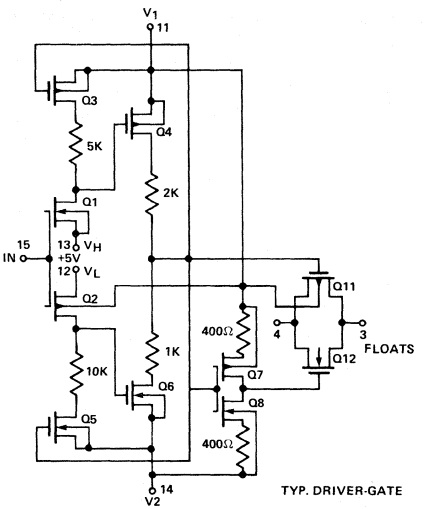
- Switches Greater Than 20Vpp Signals With ±15V Supplies
- Quiescent Current Less Than 10μA
- Overvoltage Protection to ±25V
- Break-Before-Make Switching t_{OFF} 80nsec, t_{ON} 200nsec Typical
- T^2L, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Complete Monolithic Construction

GENERAL DESCRIPTION

The IH200 solid state analog gate is designed using an improved, high voltage CMOS monolithic technology. The IH200 provides ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device. Destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The INTERSIL CMOS technology has eliminated this serious systems problem.

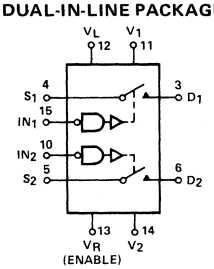
Key performance advantages of the IH200 are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 10μA. Also designed into the IH200 is guaranteed Break-Before-Make switching. This is logically accomplished by extending the t_{ON} time (200 nsec TYP.) such that it exceeds t_{OFF} time (80 nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. This eliminates the need for external logic required to avoid channel to channel shorting during switching.

FUNCTIONAL DIAGRAM



PIN CONFIGURATIONS

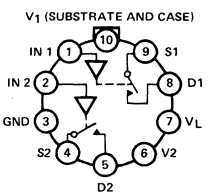
DUAL-IN-LINE PACKAGE



ORDER NUMBERS:
IH200MDE OR IH200CDE

SWITCH STATES ARE FOR LOGIC "1" INPUT

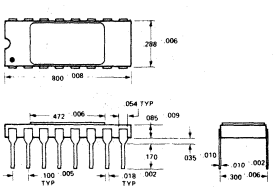
METAL CAN PACKAGE



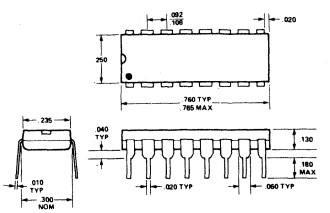
ORDER NUMBERS:
IH200AA OR IH200BA

PACKAGE DIMENSIONS

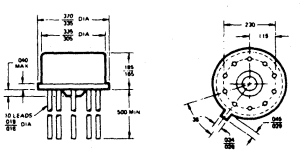
16 PIN CERAMIC PACKAGE (DE)



16 PIN DIP PACKAGE (PE)



TO-100 PACKAGE



NOTE: All dimensions in inches.

MAXIMUM RATINGS

Current (Any Terminal)	<30 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Power Dissipation	450mW
(All Leads Soldered to a P.C. Board)	
Derate 6 mW/°C Above 70°C	

$V_I - V_2$	<33V
$V_I - V_D$	<30V
$V_D - V_2$	<30V
$V_D - V_S$	<±22V
$V_L - V_2$	<33V
$V_L - V_{IN}$	<30V
$V_L - V_R$	<20V
$V_{IN} - V_R$	<20V

ELECTRICAL CHARACTERISTICS (@ 25°C, V_1 = +15V, V_2 = −15V, V_L = +5 V, V_R = 0 V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	TEST CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 0.8 V
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 2.4 V
$R_{DS(ON)}$	Drain–Source On Resistance	75	75	150	80	80	130	Ω	I_S = 1mA, V_{ANALOG} = −10 V to +10 V
$\triangle R_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = 1 mA,
V_{ANALOG}	Min. Analog Signal Handling Capability	±11	±11	±11	±10	±10	±10	V	I_S = 10 mA
$I_{D(OFF)}$	Switch OFF Leakage Current	5	5	500	5	5	250	nA	V_{ANALOG} = −10 V to +10 V
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	5	5	500	10	10	250	nA	V_D = V_S = −10 V to +10 V
t_{ON}	Switch "ON" Time		1.0			1.0		μs	R_L = 1 kΩ, V_{ANALOG} = −10 V to +10 V See Fig. A
t_{OFF}	Switch "OFF" Time		0.5			0.5		μs	R_L = 1 kΩ, V_{ANALOG} = −10 V to +10 V See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50			f = 1 MHz, R_L = 100Ω, C_L ≤5 pF See Fig. C
I_{V1}	+ Power Supply Quiescent Current	10	10	100	10	10	100	μA	
I_{V2}	− Power Supply Quiescent Current	10	10	100	10	10	100	μA	V_1 = +15 V, V_2 = −15 V, V_L = +5 V V_L = +5 V, V_R = 0
I_{VL}	+5 V Supply Quiescent Current	10	10	100	10	10	100	μA	Switch Duty Cycle <10%
I_{VR}	Gnd Supply Quiescent Current	10	10	100	10	10	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off

TEST CIRCUITS

FIG. A

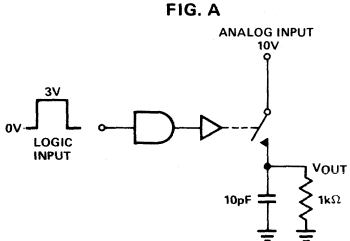


FIG. B

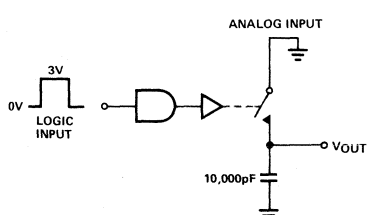
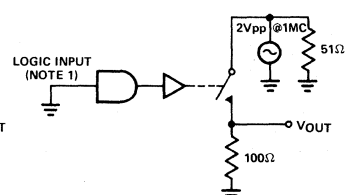


FIG. C



MILITARY SPECIFICATION
741
OPERATIONAL AMPLIFIER

JM38510/10101

SCOPE

This specification covers the detail requirements for monolithic silicon operational amplifiers. A choice of case outline and lead finish are provided for each type and are reflected in the complete part number.

PART NUMBER/ORDERING INFORMATION

The complete ordering part number is made up as shown:

*M38510	/101	01	B	A	C
Military Designator	Detail Specifications	741 Operational Amplifier	Device Class	Case Outline (Table I)	Lead Finish In Accordance With MIL-M-38510

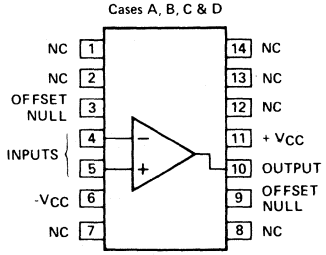
*"JAN" approved part to be ordered and marked: JM38510 - - - -

CASE OUTLINE (TABLE I)

Letter	MIL-M38510 Appendix C Case Outline	Approval
A	F-1 (14 lead, ¼" X ¼" flatpack)	N/A: Consult Factory
B	F-3 (14 lead, ¼" X 1/8" flatpack)	N/A: Consult Factory
C	D-1 (14 lead, ¼" X ¾" dual-in-line)	N/A: Consult Factory
D	F-2 (14 lead, ¼" X 3/8" flatpack)	N/A: Consult Factory
G	A-1 (8 lead can)	1976 "JAN" Part I QPL
H	F-4 (10 lead, ¼" X ¼" flatpack)	N/A: Consult Factory

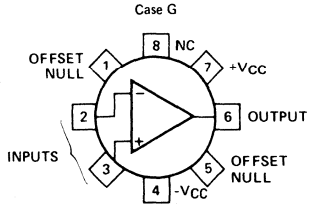
CONNECTION DIAGRAMS

Cases A, B, C & D



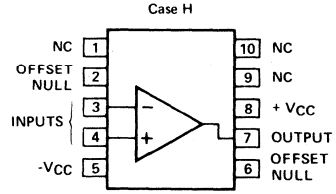
14 Lead Flat Pack or Dual-In-Line (TOP VIEW)

Case G



8 Lead Can (TOP VIEW)

Case H



10 Lead Flat Pack (TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

Supply voltage range	±22 Vdc **Note 1**
Input voltage range	±20 Vdc **Note 2**
Differential input voltage range	±30 Vdc
Input current range	-0.1 to +10 mA
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited **Note 3**
Lead temperature (soldering, 60 sec)	300° C
Junction temperature	T_J = 175° C **Note 4**

RECOMMENDED OPERATING CONDITIONS

Supply voltage range	±5 to ±20 Vdc
Ambient temperature range	-55 to + 125° C

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ J-A
14 lead FP	A, B, D	350 mW @ T_A = 125°C	60° C/W	140° C/W
Dual-in-line	C	400 mW @ T_A = 125°C	35° C/W	120° C/W
8 lead can	G	330 mW @ T_A = 125°C	40° C/W	150° C/W
10 lead FP	H	330 mW @ T_A = 125°C	60° C/W	150° C/W

Note 1 - Voltages in excess of these may be applied for short-term tests if voltage difference does not exceed 44 volts.
Note 2 - For supply voltages less than ±20 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 3 - Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
Note 4 - For short term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum) $T_J \leq 275°C$.

ELECTRICAL PERFORMANCE CHARACTERISTICS

Characteristics	Symbol	Conditions	741 -01 Min.	741 -01 Max.	Units
Input offset voltage	V_{IO}	R_S = 50Ω, T_A = 25°C	-3.0	+3.0	mV
		R_S = 50Ω, -55°C ≤ T_A ≤ 125°C	-4.0	+4.0	mV
Input offset voltage temperature sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	ΔT_A from -55°C to +25°C	-15	+15	µV/°C
		ΔT_A from +25°C to +125°C	-15	+15	µV/°C
Input offset current	I_{IO}	+25°C ≤ T_A ≤ 125°C	-30	+30	nA
		-55°C ≤ T_A < +25°C	-70	+70	nA
Input offset current temperature sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	ΔT_A from -55°C to +25°C	-500	+500	pA/°C
		ΔT_A from +25°C to +125°C	-200	+200	pA/°C
Input bias current	$+I_{IB}$	25°C ≤ T_A ≤ 125°C	+1.0	110	nA
		-55°C ≤ T_A < +25°C	+1.0	265	nA
	$-I_{IB}$	25°C ≤ T_A < 125°C	+1.0	110	nA
		-55°C ≤ T_A < +25°C	+1.0	265	nA
Power supply rejection ratio	+PSRR	$+V_{CC}$ = 10V, $-V_{CC}$ = -20V, R_S = 50Ω, T_A = 25°C	0	50	µV/V
Power supply rejection ratio	-PSRR	$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, R_S = 50Ω, T_A = 25°C	0	50	µV/V
Input voltage common mode rejection	CMR	$\pm V_{CC}$ = 20V, V_{IN} = ±15V, R_S = 50Ω	80	-	dB
Adjustment for input offset voltage	V_{IO} ADJ (+)	$\pm V_{CC}$ = 20V	7.5	-	mV

ELECTRICAL PERFORMANCE CHARACTERISTICS, Continued

Characteristics	Symbol	Conditions		Min.	Max.	Units
Adjustment for input offset voltage	V_{IO} ADJ (-)	$\pm V_{CC}$ = 20V		7.5	-	mV
Output short circuit current (for positive output)	I_{OS} (+)	$\pm V_{CC}$ = 15V	$+25^{\circ}C \leq T_A \leq +125^{\circ}C$	-40	-9	mA
			$-55^{\circ}C \leq T_A < 25^{\circ}C$	-55	-9	mA
Output short circuit current (for negative output	I_{OS} (-)	$\pm V_{CC}$ = 15V	$+25^{\circ}C \leq T_A \leq +125^{\circ}C$	9	40	mA
			$-55^{\circ}C \leq T_A < 25^{\circ}C$	9	55	mA
DC power dissipation per amplifier (Quiescent)	P_D	$\pm V_{CC}$ = 20V	$T_A = -55^{\circ}C$	10	165	mW
			$T_A = +25^{\circ}C$	10	150	mW
			$T_A = +125^{\circ}C$	10	135	mW
Single-ended input impedance (non-inverting input)	Z_{is1}	$\pm V_{CC}$ = 20V Note 5	$T_A = 25^{\circ}C$	1.0	-	MΩ
			$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	0.5	-	MΩ
Single-ended input impedance (inverting input)	Z_{is2}	$\pm V_{CC}$ = 20V Note 5	$T_A = 25^{\circ}C$	1.0	-	MΩ
			$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	0.5	-	MΩ
Output voltage swing (maximum)	V_{OPP}	$\pm V_{CC}$ = 20V, R_L = 10 kΩ		32	-	V
		$\pm V_{CC}$ = 20V, R_L = 2 kΩ		30	-	V
Open loop voltage gain (single ended) Note 6	$A_{vs}(\pm)$	$\pm V_{CC}$ = 20V, R_L = 2 kΩ, 10 kΩ, V_{OUT} = ±15V	$T_A = 25^{\circ}C$	50	-	V/mV
			$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	32	-	V/mV
Open loop voltage gain (single ended) Note 6	A_{vs} (±)	$\pm V_{CC}$ = 5V, R_L = 2 kΩ, 10 kΩ, V_{OUT} = ±2V		10	-	V/mV
Transient response	TR	Rise time		-	800	ns
Rise time		Overshoot	$T_A = -55^{\circ}C$	-	20	%
Overshoot			$T_A = 25^{\circ}C$	-	20	%
			$T_A = 125^{\circ}C$	-	20	%
Bandwidth Note 7	BW			.43	-	MHz
Slew rate	SR (+)	V_{IN} = ±5 V; A_V = 1	$25^{\circ}C \leq T_A \leq 125^{\circ}C$	0.3	-	V/μs
			$T_A = -55^{\circ}C$	0.3	-	
Slew rate	SR (-)	V_{IN} = ±5 V; A_V = 1	$25^{\circ}C \leq T_A \leq 125^{\circ}C$	0.3	-	V/μs
			$T_A = -55^{\circ}C$	0.3	-	
Noise (referred to input)	N_I	$\pm V_{CC}$ = 20 V; Bandwidth = 5 kHz		-	15	μV_{rms}
				-	40	μV_{peak}

Note 5 - Guaranteed by I_{IB} tested at common mode extremes.

Note 6 - Note that gain is not specified at V_{IO} (ADJ) extremes. Some gain reduction is usually seen at V_{IO} (ADJ) extremes. For closed loop applications (closed loop gain less than 1,000), the open loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open loop gain or open loop gain linearity), they should be specified in the individual procurement document as additional requirements.

Note 7 - Calculated value from: BW (MHz) = $\frac{0.35}{\text{Rise time } (\mu s)}$

PROCESS SCREENING REQUIREMENTS

MIL-STD-883A TEST METHODS	DESCRIPTION	JAN M38510 CLASS B	JAN M38510 CLASS C
Preseal Visual MTD. 2010	Cond. B Visual Criteria	PRESEAL VISUAL COND. B	PRESEAL VISUAL COND. B
Bond Strength	Bond strength is monitored on a sample basis two times per shift per machine	BOND STRENGTH ACCEPTANCE	BOND STRENGTH ACCEPTANCE
Seal	Devices are hermetically sealed for compliance to MIL-STD-883 requirements	SEAL	SEAL
High Temp Storage	Cond. C = 150°C	BAKE COND. C 24 HRS.	BAKE COND. C 24 HRS.
Temperature Cycle MTD 1010	Cond. C -65°/150°C 10 cycles	TEMP CYCLE COND. C	TEMP CYCLE COND. C
Constant Acceleration MTD 2001	Cond. E 30000 G's X_1	CENTRIFUGE COND. E Y_1 ONLY	CENTRIFUGE COND. E Y_1 ONLY
Hermetic Seal MTD 1014	Cond. A Fine-Helium $5x10^{-8}$ cc/sec Cond. B Fine-Radiflo $5x10^{-8}$ cc/sec Cond. C1 Gross-FC43/Hot 10^{-3} cc/sec Cond. C2 Gross-FC78/Vacuum 10^{-5} cc/sec	HERMETICITY COND. A/B COND. C1-2	HERMETICITY COND. A/B COND. C1-2
Pre Burn-in Electrical 5004	25°C dc electrical testing to remove rejects prior to submission to burn-in screen	OPTIONAL PRE B I ELECT 25°C dc	
Burn-in Screen MTD 1015	Cond. A, Cond. B, Cond C	BURN-IN 160 HRS.	
Post Burn-in Electrical 5004	Post Burn-in electrical screening to cull out devices which failed as a result of burn-in. Test Parameters may include 25°C dc, 125°C dc, -55°C dc, 25°C dc, 25°C ac and 25°C Functional tests.	PST B I ELECT 25°C dc +125°C dc -55°C dc 25°C ac	ELECTRICAL 25°C dc 25°C FUNCTIONAL
Radiography MTD 2012	6X, 8X magnification Specify number of views		
Quality Conformance Inspection MTD 5005	Group A: Electrical Characteristics Group B: Tests Group C: Die Related Tests Group D: Package Related Tests	QUALITY CONFORMANCE Gp. A, B, C & D	QUALITY CONFORMANCE Gp. A, B, C & D
External Visual MTD 2009	3X, 10X magnification. Verify dimensions configuration, lead structure, marking and workmanship	EXTERNAL VISUAL 100%	EXTERNAL VISUAL 100%

ORDERING

Part Number JM38510/10101BGC

Part Marking JM38510/10101BGC

ELECTRICAL END POINTS

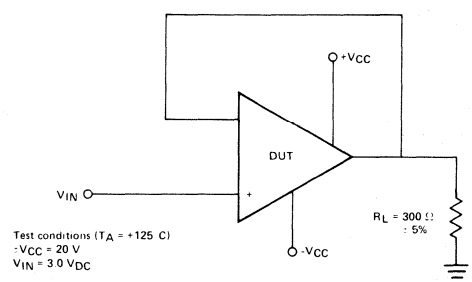
741

Test	Unit	-01 Limit Min.	-01 Limit Max.	-01 Delta* Min.	-01 Delta* Max.
V_{IO}	mV	-3.0	+3.0	-0.5	+0.5
I_{IO}	nA	-30	+30	-3	+3
$+I_{IB}$	nA	+1.0	+110	-10	+10
$-I_{IB}$	nA	+1.0	+110	-10	+10

Groups C and D, end point electrical parameters.
(T_A = 25°C, Vcc = ±20 V, Vcm = +15 V, -15 V, 0 V).

*Group C Subgroup 1 Only.

BURN-IN (STEADY STATE POWER AND REVERSE BIAS) AND OPERATING LIFE TEST



Life test cooldown procedure. When devices are measured at 25°C following application of the operating life or burn-in test condition, they shall be cooled to room temperature prior to removal of the bias.

MILITARY SPECIFICATION
LM101
OPERATIONAL AMPLIFIER

Intersil

JM38510/10103

APPROVAL PENDING

SCOPE

This specification covers the detail requirements for monolithic silicon operational amplifiers. A choice of case outline and lead finish is provided for each type and is reflected in the complete part number.

PART NUMBER/ORDERING INFORMATION

The complete ordering part number is made up as shown:

*M38510	/101	03	B	A	C
Military Designator	Detail Specifications	LM101 Operational Amplifier	Device Class	Case Outline (Table I)	Lead Finish In Accordance With MIL-M-38510

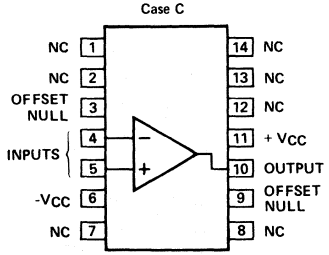
*"JAN" approved part to be ordered and marked: JM38510 - - - -

CASE OUTLINE (TABLE I)

Letter	MIL-M38510 Appendix C Case Outline	Approval
C	D-1 (14 lead, ¼" X ¾" dual-in-line)	N/A: Consult Factory
G	A-1 (8 lead can)	1976 "JAN" Part I QPL
H	F-4 (10 lead, ¼" X ¼" flatpack)	N/A: Consult Factory

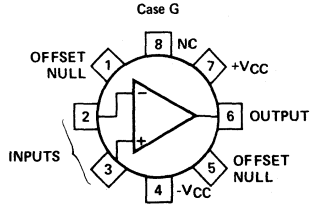
CONNECTION DIAGRAMS

Case C



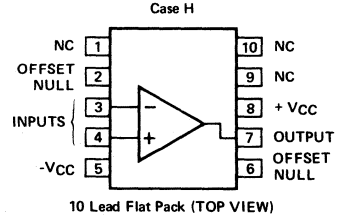
14 Lead Flat Pack or Dual-In-Line (TOP VIEW)

Case G



8 Lead Can (TOP VIEW)

Case H



10 Lead Flat Pack (TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

Supply voltage range	±22 Vdc **Note 1**
Input voltage range	±20 Vdc **Note 2**
Differential input voltage range	±30 Vdc
Input current range	-0.1 to +10 mA
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited **Note 3**
Lead temperature (soldering, 60 sec)	300° C
Junction temperature	T_J = 175° C **Note 4**

RECOMMENDED OPERATING CONDITIONS

Supply voltage range	±5 to ±20 Vdc
Ambient temperature range	-55 to + 125° C

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ J-A
Dual-in-line	C	400 mW @ T_A = 125°C	35° C/W	120° C/W
8 lead can	G	330 mW @ T_A = 125°C	40° C/W	150° C/W
10 lead FP	H	330 mW @ T_A = 125°C	60° C/W	150° C/W

Note 1 - Voltages in excess of these may be applied for short-term tests if voltage difference does not exceed 44 volts.
Note 2 - For supply voltages less than ±20 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 3 - Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
Note 4 - For short term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum) $T_J \leq 275°C$.

ELECTRICAL PERFORMANCE CHARACTERISTICS

Characteristics	Symbol	Conditions	LM101 –03 Min.	LM101 –03 Max.	Units
Input offset voltage	V_{IO}	$R_S = 50\Omega$, $T_A = 25°C$	–1.5	+1.5	mV
		$R_S = 50\Omega$, $-55°C \leq T_A \leq 125°C$	–3.0	+3.0	mV
Input offset voltage temperature sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	ΔT_A from –55°C to +25°C	–15	+15	µV/°C
		ΔT_A from +25°C to +125°C	–15	+15	µV/°C
Input offset current	I_{IO}	$+25°C \leq T_A \leq 125°C$	–10	+10	nA
		$-55°C \leq T_A < +25°C$	–20	+20	nA
Input offset current temperature sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	ΔT_A from –55°C to +25°C	–150	+150	pA/°C
		ΔT_A from +25°C to +125°C	–100	+100	pA/°C
Input bias current	$+I_{IB}$	$25°C \leq T_A \leq 125°C$	+1.0	65	nA
		$-55° \leq T_A < +25°C$	+1.0	100	nA
	$-I_{IB}$	$25°C \leq T_A < 125°C$	+1.0	65	nA
		$-55°C \leq T_A < +25°C$	+1.0	100	nA
Power supply rejection ratio	+PSRR	$+V_{CC}$ = 10V, $-V_C$ = –20V, $R_S = 50\Omega$, T_A = 25°C	0	50	µV/V
Power supply rejection ratio	–PSRR	$+V_{CC}$ = 20V, $-V_{CC}$ = –10V, $R_S = 50\Omega$, T_A = 25°C	0	50	µV/V

ELECTRICAL PERFORMANCE CHARACTERISTICS, Continued

Characteristics	Symbol	Conditions		Min.	Max.	Units
Input voltage common mode rejection	CMR	$\pm V_{CC}$ = 20V, V_{IN} = ±15V	R_S = 50Ω	90	–	dB
Adjustment for input offset voltage	V_{IO} ADJ (+)	$\pm V_{CC}$ = 20V		7.5	–	mV
Adjustment for input offset voltage	V_{IO} ADJ (–)	$\pm V_{CC}$ = 20V		7.5	–	mV
Output short circuit current (for positive output)	I_{OS} (+)	$\pm V_{CC}$ = 15V	$+25°C \leqslant T_A \leqslant +125°C$	–40	–9	mA
			$-55°C \leqslant T_A \leqslant 25°C$	–55	–9	mA
Output short circuit current (for negative output)	I_{OS} (–)	$\pm V_{CC}$ = 15V	$+25°C \leqslant T_A \leqslant +125°C$	9	40	mA
			$-55°C \leqslant T_A \leqslant 25°C$	9	55	mA
DC power dissipation per amplifier (Quiescent)	P_D	$\pm V_{CC}$ = 20V	$T_A = -55°C$	10	140	mW
			$T_A = +25°C$	10	120	mW
			$T_A = +125°C$	10	100	mW
Single-ended input impedance (non-inverting input)	Z_{is1}	$\pm V_{CC}$ = 20V **Note 5**	$T_A = 25°C$	1.5	–	MΩ
			$-55°C \leqslant T_A \leqslant +125°C$	1.0	–	MΩ
Single-ended input impedance (inverting input)	Z_{is2}	$\pm V_{CC}$ = 20V **Note 5**	$T_A = 25°C$	1.5	–	MΩ
			$-55°C \leqslant T_A \leqslant +125°C$	1.0	–	MΩ
Output voltage swing (maximum)	V_{OPP}	$\pm V_{CC}$ = 20V, R_L = 10 kΩ		32	–	V
		$\pm V_{CC}$ = 20V, R_L = 2 kΩ		30	–	V
Open loop voltage gain (single ended) **Note 6**	A_{vs} (±)	$\pm V_{CC}$ = 20V, R_L = 2 kΩ, 10 kΩ, V_{OUT} = ±15V	$T_A = 25°C$	100	–	V/mV
			$-55°C \leqslant T_A \leqslant +125°C$	50	–	V/mV
Open loop voltage gain (single ended) **Note 6**	A_{vs} (±)	$\pm V_{CC}$ = 5V, R_L = 2 kΩ, 10 kΩ, V_{OUT} = ±2V		10	–	V/mV
Transient response	TR	Rise time		–	800	ns
Overshoot			$T_A = -55°C$	–	20	%
			$T_A = 25°C$	–	20	%
			$T_A = 125°C$	–	25	%
Bandwidth **Note 7**	BW			0.43	–	MHz
Slew rate	SR (+)	V_{IN} = ±5V; A_V = 1	$25°C \leqslant T_A \leqslant 125°C$	0.3	–	V/μs
			$T_A = -55°C$	0.2	–	V/μs
		V_{IN} = ±1.0V; A_V = 10	$25°C \leqslant T_A \leqslant 125°C$	3.0	–	V/μs
			$T_A = -55°C$	2.0	–	V/μs
Slew Rate	SR (–)	V_{IN} = ±5V; A_V = 1	$25°C \leqslant T_A \leqslant 125°C$	0.3	–	V/μs
			$T_A = -55°C$	0.2	–	V/μs
		V_{IN} = ±1.0; A_V = 10	$-55°C \leqslant T_A \leqslant 125°C$	3.0	–	ns
			$T_A = -55°C$	2.0	–	ns
Noise (referred to input)	N_I	$\pm V_{CC}$ = 20V; Bandwidth = 5 kHz		–	10	μVrms
				–	30	μVpeak

Note 5 - Guaranteed by I_{IB} tested at common mode extremes.

Note 6 - Note that gain is not specified at V_{IO} (ADJ) extremes. Some gain reduction is usually seen at V_{IO} (ADJ) extremes. For closed loop applications (closed loop gain less than 1,000), the open loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open loop gain or open loop gain linearity), they should be specified in the individual procurement document as additional requirements.

Note 7 - Calculated value from: BW (MHz) = $\frac{0.35}{\text{Rise time } (\mu s)}$

PROCESS SCREENING REQUIREMENTS

MIL-STD-883A TEST METHODS	DESCRIPTION	JAN M38510 CLASS B	JAN M38510 CLASS C
Preseal Visual MTD. 2010	Cond. B Visual Criteria	PRESEAL VISUAL COND. B	PRESEAL VISUAL COND. B
Bond Strength	Bond strength is monitored on a sample basis two times per shift per machine	BOND STRENGTH ACCEPTANCE	BOND STRENGTH ACCEPTANCE
Seal	Devices are hermetically sealed for compliance to MIL-STD-883 requirements	SEAL	SEAL
High Temp Storage	Cond. C = 150°C	BAKE COND. C 24 HRS.	BAKE COND. C 24 HRS.
Temperature Cycle MTD 1010	Cond. C -65°/150°C 10 cycles	TEMP CYCLE COND. C	TEMP CYCLE COND. C
Constant Acceleration MTD 2001	Cond. E 30000 G's X_1	CENTRIFUGE COND. E Y_1 ONLY	CENTRIFUGE COND. E Y_1 ONLY
Hermetic Seal MTD 1014	Cond. A Fine-Helium $5x10^{-8}$ cc/sec Cond. B Fine-Radiflo $5x10^{-8}$ cc/sec Cond. C1 Gross-FC43/Hot 10^{-3} cc/sec Cond. C2 Gross-FC78/Vacuum 10^{-5} cc/sec	HERMETICITY COND. A/B COND. C1-2	HERMETICITY COND. A/B COND. C1-2
Pre Burn-in Electrical 5004	25°C dc electrical testing to remove rejects prior to submission to burn-in screen	OPTIONAL PRE B/I ELECT 25°C dc	
Burn-in Screen MTD 1015	Cond. A, Cond. B, Cond C	BURN-IN 160 HRS.	
Post Burn-in Electrical 5004	Post Burn-in electrical screening to cull out devices which failed as a result of burn-in. Test Parameters may include: 25°C dc, 125°C dc, -55°C dc, 25°C dc, 25°C ac and 25°C Functional tests.	PST B/I ELECT 25°C dc +125°C dc -55°C dc 25°C ac	ELECTRICAL 25°C dc 25°C FUNCTIONAL
Radiography MTD 2012	6X, 8X magnification Specify number of views		
Quality Conformance. Inspection MTD 5005	Group A: Electrical Characteristics Group B: Tests Group C: Die Related Tests Group D: Package Related Tests	QUALITY CONFORMANCE Gp. A, B, C & D	QUALITY CONFORMANCE Gp. A, B, C & D
External Visual MTD 2009	3X, 10X magnification: Verify dimensions configuration, lead structure, marking and workmanship	EXTERNAL VISUAL 100%	EXTERNAL VISUAL 100%

ORDERING		
	Part Number	JM38510/ 10103BGC
	Part Marking	JM38510/ 10103BGC

ELECTRICAL END POINTS

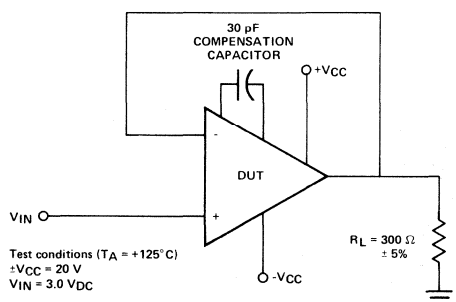
LM101

Test	Unit	–03			
		Limit		Delta*	
		Min.	Max.	Min.	Max.
V_{IO}	mV	–1.5	+1.5	–0.4	+0.4
I_{IO}	nA	–10	+10	–2	+2
$+I_{IB}$	nA	+1.0	+55	–6.5	+6.5
$-I_{IB}$	nA	+1.0	+65	–6.5	+6.5

Groups C and D, end point electrical parameters.
(T_A = 25°C, Vcc = ±20 V, Vcm = +15 V, -15 V, 0 V).

*Group C Subgroup 1 Only.

BURN-IN (STEADY STATE POWER AND REVERSE BIAS) AND OPERATING LIFE TEST



Life test cooldown procedure. When devices are measured at 25°C following application of the operating life or burn-in test condition, they shall be cooled to room temperature prior to removal of the bias.

MILITARY SPECIFICATION
LM108
OPERATIONAL AMPLIFIER

JM38510/10104

APPROVAL PENDING

SCOPE

This specification covers the detail requirements for monolithic silicon operational amplifiers. A choice of case outline and lead finish is provided for each type and is reflected in the complete part number.

PART NUMBER/ORDERING INFORMATION

The complete ordering part number is made up as shown:

*M38510	/101	04	B	A	C
Military Designator	Detail Specifications	LM108 Operational Amplifier	Device Class	Case Outline (Table I)	Lead Finish In Accordance With MIL-M-38510

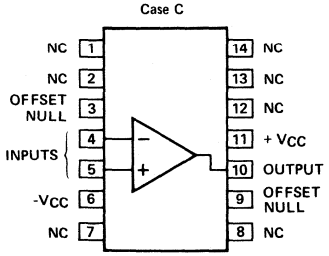
*"JAN" approved part to be ordered and marked: JM38510 - - - -

CASE OUTLINE (TABLE I)

Letter	MIL-M38510 Appendix C Case Outline	Approval
C	D-1 (14 lead, ¼" X ¾" dual-in-line)	N/A: Consult Factory
G	A-1 (8 lead can)	1976 "JAN" Part I QPL
H	F-4 (10 lead, ¼" X ¼" flatpack)	N/A: Consult Factory

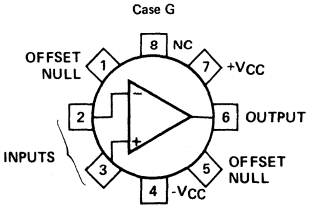
CONNECTION DIAGRAMS

Case C



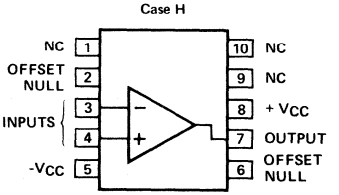
14 Lead Flat Pack or Dual-In-Line (TOP VIEW)

Case G



8 Lead Can (TOP VIEW)

Case H



10 Lead Flat Pack (TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

Supply voltage range	±22 Vdc **Note 1**
Input voltage range	±20 Vdc **Note 2**
Differential input voltage range	±30 Vdc **Note 3**
Input current range	-0.1 to +10 mA
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited **Note 4**
Lead temperature (soldering, 60 sec)	300° C
Junction temperature	T_J = 175°C **Note 5**

RECOMMENDED OPERATING CONDITIONS

Supply voltage range	±5 to ±20 Vdc
Ambient temperature range	-55 to + 125° C

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ J-A
Dual-in-line	C	400 mW @ T_A = 125°C	35° C/W	120° C/W
8 lead can	G	330 mW @ T_A = 125°C	40° C/W	150° C/W
10 lead FP	H	330 mW @ T_A = 125°C	60° C/W	150° C/W

Note 1 - Voltages in excess of these may be applied for short-term tests if voltage difference does not exceed 44 volts.
Note 2 - For supply voltages less than ±20 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 3 - Resistance of 10 kΩ or greater must be inserted in series with the inputs to limit current in the input shunt diodes to the maximum allowable value.
Note 4 - Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
Note 5 - For short term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum) $T_J \leq 275°C$.

ELECTRICAL PERFORMANCE CHARACTERISTICS

Characteristics	Symbol	Conditions	LM108 –04 Min.	LM108 –04 Max.	Units
Input offset voltage	V_{IO}	R_S = 50Ω, T_A = 25°C	–0.5	+0.5	mV
		R_S = 50Ω, –55°C ≤ T_A ≤ 125°C	–1.0	+1.0	mV
Input offset voltage temperature sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	ΔT_A from –55°C to +25°C	–5.0	+5.0	μV/°C
		ΔT_A from +25°C to +125°C	–5.0	+5.0	μV/°C
Input offset current	I_{IO}	T_A = +25°C	–0.2	+0.2	nA
		–55°C ≤ T_A < +125°C	–0.4	+0.4	nA
Input offset current temperature sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	ΔT_A from –55°C to +25°C	–2.5	+2.5	pA/°C
		ΔT_A from +25°C to +125°C	–2.4	+2.4	pA/°C
Input bias current	$+I_{IB}$	25°C ≤ T_A ≤ 125°C	–2.0	+2.0	nA
		–55°C ≤ T_A < +25°C	–0.1	+3.0	nA
	$-I_{IB}$	25°C ≤ T_A < 125°C	–2.0	+2.0	nA
		–55°C ≤ T_A < +25°C	–0.1	+3.0	nA
Power supply rejection ratio	+PSRR	$+V_{CC}$ = 10V, $-V_{CC}$ = –20V, R_S = 50Ω, T_A = 25°C	0	16	μV/V
Power supply rejection ratio	–PSRR	$+V_{CC}$ = 20V, $-V_{CC}$ = –10V, R_S = 50Ω, T_A = 25°C	0	16	μV/V

ELECTRICAL PERFORMANCE CHARACTERISTICS, Continued

Characteristics	Symbol	Conditions		Min.	Max.	Units
Input voltage common mode rejection	CMR	$\pm V_{CC}$ = 20V V_{IN} = ±15V	R_S = 50Ω	96	–	dB
Output short circuit current (for positive output)	I_{OS} (+)	$\pm V_{CC}$ = 15V	+25°C ≤ T_A ≤ +125°C	–15	–2.0	mA
			–55°C ≤ T_A < 25°C	–15	–4.0	mA
Output short circuit current (for negative output)	I_{OS} (–)	$\pm V_{CC}$ = 15V	+25°C ≤ T_A ≤ +125°C	2.0	15	mA
			–55°C ≤ T_A < 25°C	4.0	15	mA
DC power dissipation per amplifier (Quiescent)	P_D	$\pm V_{CC}$ = 20V	T_A = –55°C	2	32	mW
			T_A = +25°C	2	24	mW
			T_A = +125°C	2	16	mW
Single-ended input impedance (non-inverting input)	Z_{is1}	$\pm V_{CC}$ = 20V **Note 6**	T_A = 25°C	20	–	MΩ
			–55°C ≤ T_A ≤ +125°C	10	–	MΩ
Single-ended input impedance (inverting input)	Z_{is2}	$\pm V_{CC}$ = 20V **Note 6**	T_A = 25°C	20	–	MΩ
			–55°C ≤ T_A ≤ +125°C	10	–	MΩ
Output voltage swing (maximum)	V_{OPP}	$\pm V_{CC}$ = 20V, R_L = 10 kΩ		32	–	V
Open loop voltage gain (single ended) **Note 7**	A_{vs} (±)	$\pm V_{CC}$ = 20V R_L = 10 kΩ V_{OUT} = ±15V	T_A = 25°C	80	–	V/mV
			–55°C ≤ T_A ≤ +125°C	40	–	V/mV
Open loop voltage gain (single ended) **Note 7**	A_{vs} (±)	$\pm V_{CC}$ = 5V R_L = 10 kΩ V_{OUT} = ±2V		20	–	V/mV
Transient response Rise time Overshoot	T_R	Rise time		–	1000	ns
		Overshoot	T_A = –55°C	–	40	%
			T_A = 25°C	–	40	%
			T_A = 125°C	–	40	%
Bandwidth **Note 8**	BW			0.35	–	MHz
Slew rate	SR (+)	V_{IN} = ±5V; A_V = 1	25°C ≤ T_A ≤ 125°C	0.1	–	V/μs
			T_A = –55°C	0.08	–	
Slew rate	SR (–)	V_{IN} = ±5V; A_V = 1	25°C ≤ T_A ≤ 125°C	0.1	–	V/μs
			T_A = –55°C	0.08	–	

Note 6 - Guaranteed by I_{IB} tested at common mode extremes.

Note 7 - Note that gain is not specified at V_{IO} (ADJ) extremes. Some gain reduction is usually seen at V_{IO} (ADJ) extremes. For closed loop applications (closed loop gain less than 1,000), the open loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open loop gain or open loop gain linearity), they should be specified in the individual procurement document as additional requirements.

Note 8 - Calculated value from: BW (MHz) = $\frac{0.35}{\text{Rise time } (\mu s)}$

PROCESS SCREENING REQUIREMENTS

MIL-STD-883A TEST METHODS	DESCRIPTION	JAN M38510 CLASS B	JAN M38510 CLASS C
Preseal Visual MTD. 2010	Cond. B Visual Criteria	PRESEAL VISUAL COND. B	PRESEAL VISUAL COND. B
Bond Strength	Bond strength is monitored on a sample basis two times per shift per machine	BOND STRENGTH ACCEPTANCE	BOND STRENGTH ACCEPTANCE
Seal	Devices are hermetically sealed for compliance to MIL-STD-883 requirements	SEAL	SEAL
High Temp Storage	Cond. C = 150°C	BAKE COND. C 24 HRS.	BAKE COND. C 24 HRS.
Temperature Cycle MTD 1010	Cond. C -65°/150°C 10 cycles	TEMP CYCLE COND. C	TEMP CYCLE COND. C
Constant Acceleration MTD 2001	Cond. E 30000 G's X_1	CENTRIFUGE COND. E Y_1 ONLY	CENTRIFUGE COND. E Y_1 ONLY
Hermetic Seal MTD 1014	Cond. A Fine-Helium $5x10^{-8}$ cc/sec Cond. B Fine-Radiflo $5x10^{-8}$ cc/sec Cond. C1 Gross-FC43/Hot 10^{-3} cc/sec Cond. C2 Gross-FC78/Vacuum 10^{-5} cc/sec	HERMETICITY COND. A/B COND. C1-2	HERMETICITY COND. A/B COND. C1-2
Pre Burn-in Electrical 5004	25°C dc electrical testing to remove rejects prior to submission to burn-in screen	OPTIONAL PRE B/I ELECT 25°C dc	
Burn-in Screen MTD 1015	Cond. A, Cond. B, Cond C	BURN-IN 160 HRS.	
Post Burn-in Electrical 5004	Post Burn-in electrical screening to cull out devices which failed as a result of burn-in. Test Parameters may include: 25°C dc, 125°C dc, -55°C dc, 25°C dc, 25°C ac and 25°C Functional tests.	PST B/I ELECT 25°C dc +125°C dc -55°C dc 25°C ac	ELECTRICAL 25°C dc 25°C FUNCTIONAL
Radiography MTD 2012	6X, 8X magnification Specify number of views		
Quality Conformance. Inspection MTD 5005	Group A: Electrical Characteristics Group B: Tests Group C: Die Related Tests Group D: Package Related Tests	QUALITY CONFORMANCE Gp. A, B, C & D	QUALITY CONFORMANCE Gp. A, B, C & D
External Visual MTD 2009	3X, 10X magnification: Verify dimensions configuration, lead structure, marking and workmanship	EXTERNAL VISUAL 100%	EXTERNAL VISUAL 100%

ORDERING **Part Number** JM38510/10104BGC

Part Marking JM38510/10104BGC

ELECTRICAL END POINTS

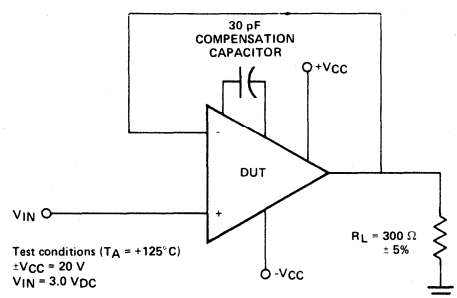
LM108

Test	Unit	–04 Limit Min.	–04 Limit Max.	–04 Delta* Min.	–04 Delta* Max.
V_{IO}	mV	–0.5	+0.5	–0.25	+0.25
I_{IO}	nA	–0.2	+0.2	–0.1	+0.1
$+I_{IB}$	nA	–0.1	+2.0	–0.2	+0.2
$-I_{IB}$	nA	–0.1	+2.0	–0.2	+0.2

Groups C and D, end point electrical parameters.
(T_A = 25°C, Vcc = ±20 V, Vcm = +15 V, -15 V, 0 V).

*Group C Subgroup 1 Only.

BURN-IN (STEADY STATE POWER AND REVERSE BIAS) AND OPERATING LIFE TEST



Life test cooldown procedure. When devices are measured at 25°C following application of the operating life or burn-in test condition, they shall be cooled to room temperature prior to removal of the bias.

LD110/LD111 3½ DIGIT A/D CONVERTER SET
LD114 MULTIPLE-OPTION DIGITAL PROCESSOR

Intersil

LD110
LD111
LD114

FEATURES

- Accuracy 0.05% Of Reading ±1 Count
- Two Voltage Ranges – 1.999 V and 199.9 mV
- Sampling Rates up to 12 Samples/Second
- FET Input for $Z_{in} > 1000\ M\Omega$
- Auto-Zero Minimizes Effects of Offset, Drift and Temperature
- Auto-Polarity
- Multiplexed Parallel BCD or Serial BCD Output (LD114)
- Active High or Active Low Logic Outputs (LD114)
- Overrange and Underrange Signals Available for Auto-Ranging Capability.
- ÷512 Output Available for Phase Locked Loop Clock (LD114)
- TTL Compatible Outputs

GENERAL DESCRIPTION

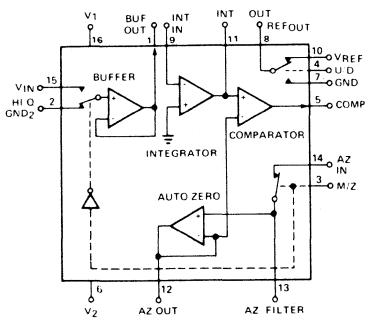
The monolithic LD111 analog processor contains a bipolar comparator, a bipolar integrating amplifier, two MOS-FET input unity gain amplifiers, several P-channel enhancement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be directly interfaced. A wide range of conversion rates (1/3 to 12 samples per second) as well as two voltage ranges can be accommodated using externally determined RC time constants. All amplifiers are internally compensated.

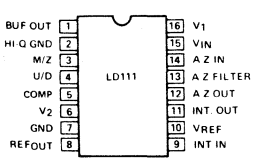
The PMOS LD110/LD114 synchronous digital processor combines the counting, storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing function of the analog processor. Seventeen static latches store the 3½ digits of BCD data as well as overrange, underrange and polarity information.

In the LD110, nine push-pull output buffers (capable of driving one standard TTL load each) provide the sign, digit strobe and multiplexed BCD data outputs, all of which are active high. The digit scan is an interlaced format of digits 1, 3, 2, and 4.

In the LD114, ten push-pull output buffers (capable of driving one standard TTL load) provide the clock frequency ÷512, sign, digit strobe and multiplexed BCD data. Four data output format options allow the user to tailor the BCD output to his circuit requirements.

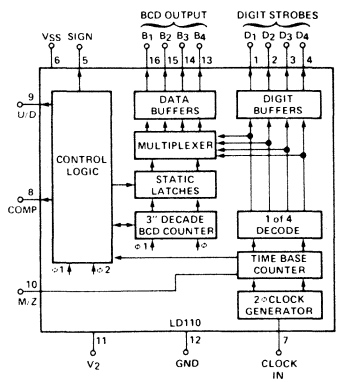
LD111 ANALOG PROCESSOR

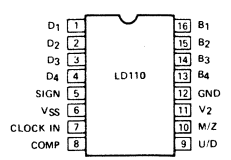




TOP VIEW

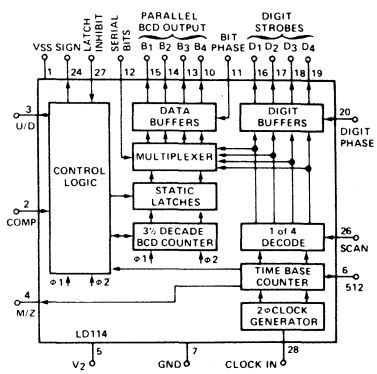
LD110 DIGITAL PROCESSOR

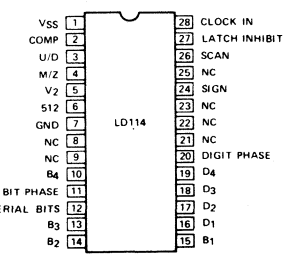




TOP VIEW

LD114 DIGITAL PROCESSOR





TOP VIEW

ABSOLUTE MAXIMUM RATINGS

V_{IN} . . . . . ±5.0V
$V_1 - V_2$ (LD111) 30V
V_{SS} 6V
$V_{SS} - V_2$ (LD110/LD114) 20V
Voltage on any pin relative to V_{SS} (LD114) 0.3 V to -20V
V_{REF} . . . . . V_1

Operating Temperature . . . . . 0 to 70°C
Storage Temperature . . . . . -65 to 150°C
Power Dissipation (Package, LD110/LD111*. . . 750 mW
Power Dissipation (Package, LD114)* . . . . 1200 mW

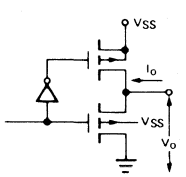
*Device mounted with all leads welded or soldered to PC Board, Derate 6.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS $V_1 = 12$ V, $V_2 = -12$ V, $V_{SS} = 5$ V $V_{REF} = 8.2$ V. $T_A = 25°C$

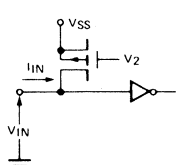
	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT	Clock Frequency	f_{IN}	50% Duty Cycle		30.7		KHz
	Input Bias Current	I_{IN}	$T_A = 25°C$		4		pA
			$T_A = 70°C$		40		
	Normal Mode Rejection	NMR	$f_L = 60$ Hz		40		dB
	Clock Input Current, Low	I_{CL}	$V_{CLOCK\ in} = 0.4$ V			-500	µA
	Comparator	I_{INL}	$V_{INL} = -12$ V			-100	
	Latch Inhibit	I_{INL}	$V_{INL} = -12$ V		180	-600	
	Format Option Inputs	I_{INH}	$V_{INH} = V_{SS}$		25	400	
OUTPUT	Measure/Zero Voltage, Low	V_{OL1}	$I_{OL} = 150\ \mu A$			0.4	V
	Measure/Zero Voltage, High	V_{OH1}	$I_{OH} = -200\ \mu A$	2.4			
	Up/Down Logic Voltage, Low	V_{OL2}	$I_{OL} = 250\ \mu A$			0.4	
	Up/Down Logic Voltage, High	V_{OH2}	$I_{OH} = -200\ \mu A$	2.4			
	Digits, Bits, Sign Voltage, ÷512*	V_{OL3}	$I_{OL} = 1.6$ mA			0.4	
	Analog Comparator Voltage	V_{OH3}	$I_{OH} = -100\ \mu A$	2.4			
	Data Bit Voltage, High	V_{OH4}	$I_{OH} = -200\ \mu A$	2.4			
	Digits, Sign Voltage, ÷512*	V_{OH5}	$I_{OH} = -800\ \mu A$	2.4			
SWITCH	ON Resistance, Auto Zero Switch	$r_{DS(on)}$	$V_{AZ(in)} = -4.0$ V, $I_S = -50\ \mu A$		11	50	KΩ
	ON Resistance, Up/Down Switch	$r_{DS(on)}$	$I_S = 1$ mA		650	3000	Ω
	Up/Down Switch Temperature Coefficient	TC			0.20	0.50	%/°C
SUPPLY	Supply Current, LD111	I_1			2.2	3.5	mA
	Supply Current, LD111	I_{2A}			-1.8	-3.0	
	Supply Current, LD110/114	I_{2D}			-17	-23	
	Supply Current, LD110/114	I_{SS}			17.4	24	
	Power Supply Rejection Ratio, V_1	$PSRR_1$		80	85		dB
	Power Supply Rejection Ratio, V_2	$PSRR_2$		60	65		
	Reference Current Rejection Ratio		$R_{REF} = R_2 = 100K\Omega$, $V_{IN} = 2$V	35	41		nA/LSB

*÷512 output applicable to LD114 only

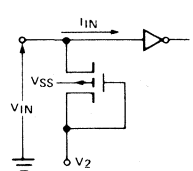
INPUT/OUTPUT SCHEMATICS



OUTPUT BUFFERS
(Digits, Bits, Sign, 512, M/Z, U/D)



COMPARATOR, CLOCK, LATCH INHIBIT INPUTS



FORMAT OPTION INPUTS
(Bit Phase, Digit Phase, Scan, Serial Bits)

DESCRIPTION OF PIN FUNCTIONS (LD110/LD114)

V_{SS} – Positive Supply Voltage. Recommended level is +5 volts ±10%.

V_2 – Negative Supply Voltage. Recommended level is -12 volts ±10%.

CLOCK IN – This input accepts a TTL or MOS level clock to drive the synchronous digital circuitry. Acceptable duty cycles on the external clock range from 30% high, 70% low to 70% high, 30% low for clock frequencies from 2 kHz to 75 kHz. Although any clock frequency between 2 kHz and 75 kHz may be used, clock frequencies that are integer divisions of $2048F_L$ ($F_{IN} = 2084F_L/n$, n = 2, 3, 4, 51, F_L = Line Frequency) provide measure and zero periods that are integer multiples of the line frequency period ($T_{zero} = n/F_L$, $T_{measure} = 2n/F_L$). Line frequency interference is minimized by the selection of one of these 50 frequencies.

This input has an active pull-up to V_{SS}.

M/Z – Measure/Zero Logic Output. This 0 to 5 volt logic output successively provides Autozero and Measurement intervals of 2048 and 4096 clock periods respectively. This output is compatible with CMOS logic and directly interfaces with the LD111 analog processor.

÷512 (LD114) – This TTL compatible output (1 standard load) provides the necessary clock frequency division for a phase locked loop digital clock. The line frequency rejection will be held at the maximum level (>80 dB) when locked to the line frequency.

U/D – Up/Down Logic Output. This output has logic levels of 0 to +5 volts to provide pulse-width modulation of the reference current when used with the LD111 analog processor. This output is CMOS compatible.

COMP – Analog Comparator Input. This input has an active pull-up to V_{SS} for a comparator "high" state. This pin must be pulled down to V_2 for a "low" comparator state.

An End-of-Conversion Signal can be decoded from the three interconnecting logic lines (M/Z, U/D, Comp) using the following CMOS logic.

$\overline{M/Z + U/D + Comp}$ - E.O.C.

SIGN – Sign of Analog Input Polarity. This TTL level output is a static signal which is either 0 or V_{SS} for a negative or positive input polarity respectively.

BIT PHASE (*LD114) – The bit outputs will be active high (positive) logic if this pin is left open or connected to V_2. The application of V_{SS} to this pin will give a complemented output (negative logic).

DIGIT PHASE (*LD114) – The Digit Strobe outputs will be of positive logic if this pin is left open or connected to V_2 (an active pull-down is internally connected to V_2). Applying V_{SS} to this pin will complement the outputs to give negative logic. Negative logic may simplify interfacing with Common Anode LED, Gas Discharge and Liquid Crystal Displays.

B_1, B_2, B_3, B_4 – BCD Data Bit Output. B_4 represents the most significant bit and B_1 the least significant bit of the BCD output. Bit 4 of digit 4 goes high for an underrange condition (less than 100 counts). These outputs are compatible with 1 standard TTL load.

MUX Underrange = $B_4 \cdot D_4$ (5% of full scale)

D_1, D_2, D_3, D_4 – Digit Strobe Outputs. D_4 is the most significant and D_1 the least significant digit of the 3½ digit output. The digit strobes are each selected in turn when the BCD data bits for that digit appear at the bit outputs.

MUX Overrange = $\overline{D_1 + D_2 + D_3 + D_4}$ (100% of full scale, count ⩾2000).

SCAN (*LD114) – Sequential/Interlace Digit Scan. The digit strobe format will be an interlaced format of digits 1, 3, 2 and 4 if this pin is left open or is connected to V_2. This format is useful for display digits packaged two to an envelope and which require an interdigit blanking period eg. (Beckman Displays). By alternating from envelope, an interdigit blanking period is effectively provided.

The application of V_{SS} to this pin will give a sequential scan of digits 1, 2, 3 and 4. This format may be more useful in interfacing with data acquisition equipment.

LATCH INHIBIT (*LD114) – Connecting this pin to V_2 will prevent updating of the internal static latches, thus providing a "hold" function. Leaving this pin disconnected will allow the latches to be updated once each sampling period.

DESCRIPTION OF PIN FUNCTIONS (LD110/LD114) Cont.

SERIAL BITS (*LD114) – Parallel/Serial Bit Output Format. The BCD data bits for each digit will appear simultaneously with the digit strobe if the parallel bit option is selected.

This format is useful for driving multiplexed displays. The parallel bit format is available when this pin is left open or connected to V_2.

The application of V_{SS} to this pin will put all of the BCD data bits in a serial order at the bit 4 output.

Bit outputs 1, 2, and 3 contain time markers to identify the data. The most significant bit of the last digit (D_4) is identified by a marker at the bit 2 output. The least significant bit of the first Digit (D_1) is identified by a marker at bit 3. Bit 1 shows a marker for the least significant bit of each digit.

All output format options are independent of one another (i.e., the serial bit output can have either sequential or interlace scan, Positive or Negative logic).

(*For LD110, action is described for "pin left open".)

DESCRIPTION OF PIN FUNCTIONS – LD111

BUF OUT – The output of this unity gain input buffer amplifier is applied to the integrator summing node through a scaling resistor R_2. The value of this resistor is typically 10 KΩ for a 200.0 mV full-scale and 100 KΩ for a 2.000 V full-scale. The digital output is inversely proportional to the value of this resistor,

$$\text{Count} = \frac{V_{IN}}{V_{REF}} \frac{R_1}{R_2} 8192$$

HI-QUALITY GND – This pin, typically connected to a High Quality Ground point for single ended inputs **CAN BE USED AS THE INVERTING INPUT FOR DIFFERENTIAL SIGNALS.** The digital output will be $V_{IN} - V_{HI} - Q$. When using this differential mode, it is important that resistor R_3 equal Resistor R_2 for proper operation.

M/Z – Measure/Zero Logic Input. Internal level shifting drivers operate the PMOS switches in response to this digital signal.

U/D – Up/Down Logic Input. The logic signal applied to this pin operates a SPDT switch to provide Quantized pulses of charge to the integrator.

COMP – This analog comparator output is an open collector configuration which goes to V_2 when "low."

V_2 – Negative Supply Voltage. Recommended level is -12 V ±10%.

GND – Analog Processor Ground.

REF_{out} – This voltage output of the SPDT U/D switch, converted to a current by resistor R_1, supplies the reference current to the integrator.

INT. IN – Integrator Summing Node.

V_{REF} – A stable positive reference voltage (5 to 11 V) applied to this pin is the standard to which the input voltage V_{IN} is measured. Ratio measurements can be made by applying a variable to this input (1.0 to 11V).

INT. OUT – The output of the integrating amplifier is made available for application to the Auto-Zero amplifier by means of resistor R_4.

AZ OUT – The output of the unity gain Auto-Zero Amplifier provides a second negative reference current to the integrator through resistor R_3.

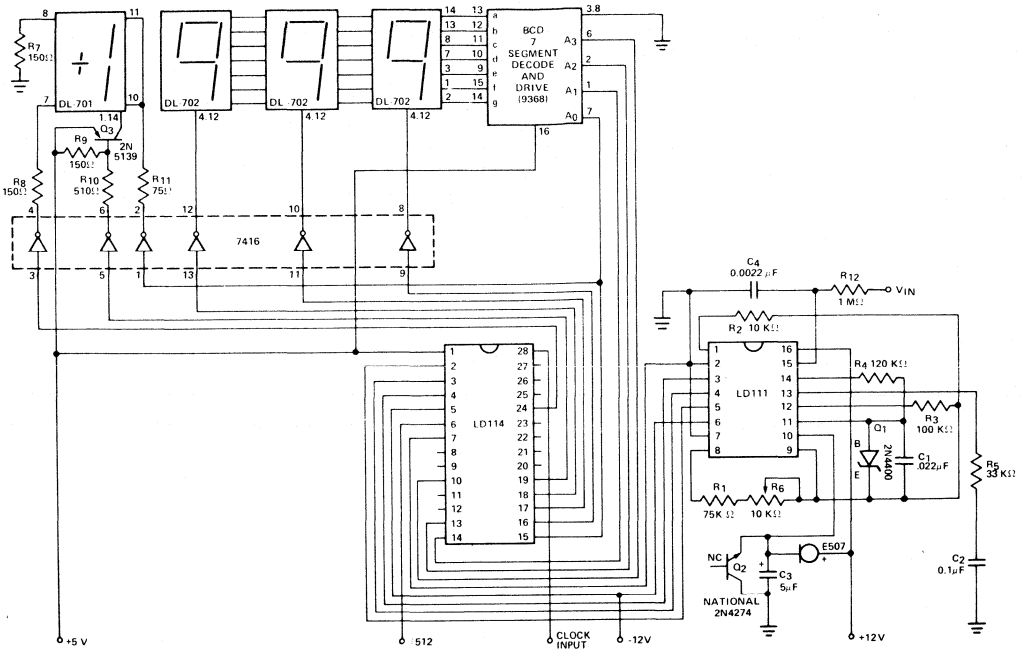
AZ FILTER – The RC filter (R_5 and C_{STRG}) connected to this pin stores. D.C. voltage components to balance amplifier offset and drift components.

AZ IN – This input is switched into the AZ filter during the Zeroing interval.

V_{IN} – Analog Voltage Input. The A/D System digitizes the voltage appearing at this input.

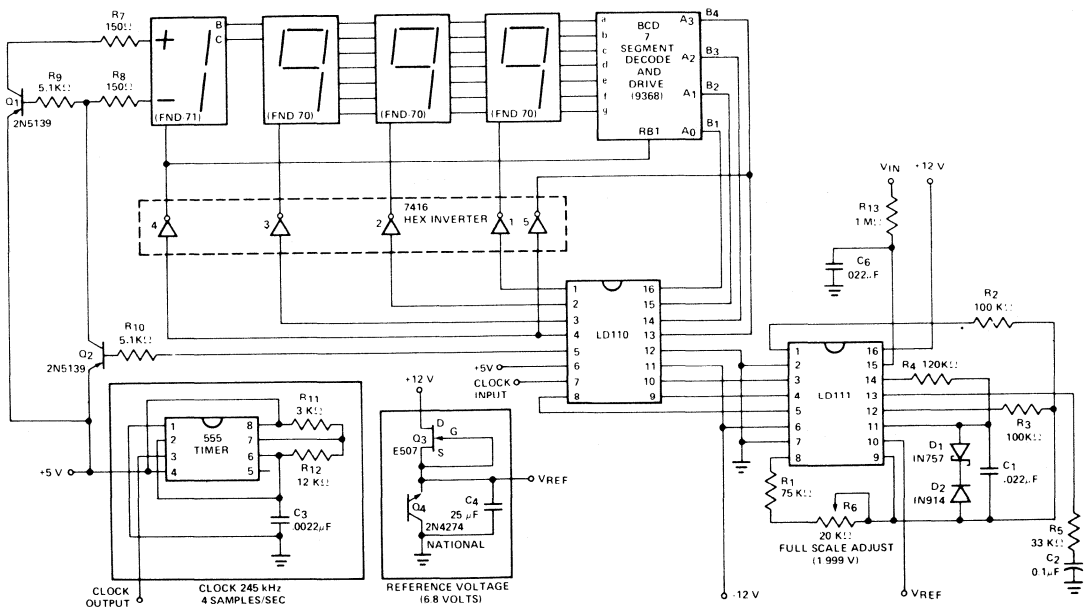
V_1 – Positive Supply Voltage. The recommended level is +12 volts ±10%.

APPLICATIONS LD111/LD114



3½ Digit DVM (±200.0 mV)

APPLICATIONS LD110/LD111



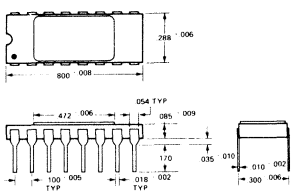
3½ Digit DVM (±2.000 Volts)

ORDERING INFORMATION

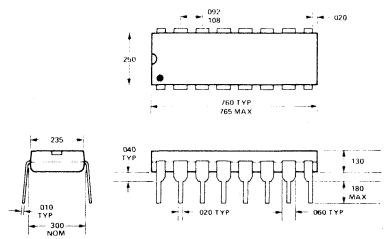
PART	TEMP. RANGE	PACKAGE	ORDER NO.
LD110	0°C to 70°C	16 lead DIP ceramic	LD110 CP
LD110	0°C to 70°C	16 lead DIP plastic	LD110 CJ
LD111	0°C to 70°C	16 lead DIP ceramic	LD111 CP
LD111	0°C to 70°C	16 lead DIP plastic	LD111 CJ
LD114	0°C to 70°C	28 lead DIP ceramic	LD114 CR

PACKAGE DIMENSIONS

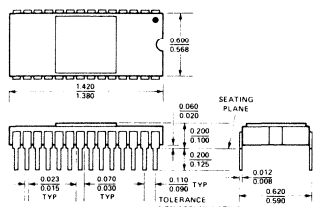
16 PIN CERAMIC PACKAGE



16 PIN DIP PACKAGE



28 LEAD DUAL-IN-LINE PACKAGE (SIDE BRAZE)



LF155, LF155A, LF255, LF355, LF355A LOW SUPPLY CURRENT
LF156, LF156A, LF256, LF356, LF356A WIDE BAND
LF157, LF157A, LF257, LF357, LF357A WIDE BAND UNCOMPENSATED ($A_{V_{MIN}}$=5)

LF155
LF156
LF157

COMMON FEATURES
(LF155A, LF156A, LF157A)

- Low input bias current — 30 pA
- Low Input Offset Current — 3 pA
- High input impedance — $10^{12}\Omega$
- Low input offset voltage — 1 mV
- Low input offset voltage temperature drift — $3\mu V/^{\circ}C$
- Low input noise current — 0.01 $pA/\sqrt{Hz}$
- High common-mode rejection ratio — 100 dB
- Large dc voltage gain — 106 dB

UNCOMMON FEATURES

	LF155A	LF156A	LF157A (A_V=5)	UNITS
Extremely fast settling time to 0.01%	4	1.5	1.5	μs
Fast slew rate	5	12	50	$V/\mu s$
Wide gain bandwidth	2.5	5	20	MHz
Low input noise voltage	20	12	12	$nV/\sqrt{Hz}$

APPLICATIONS

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

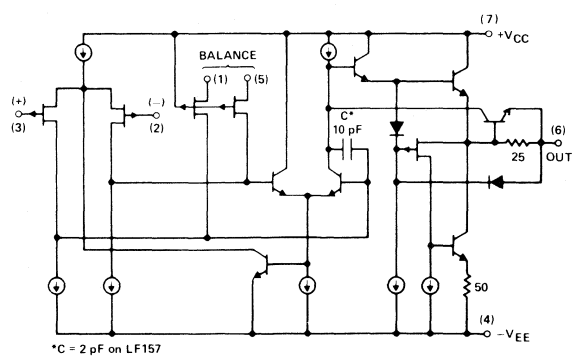
GENERAL DESCRIPTION

These monolithic JFET input operational amplifiers incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BIFET Technology). These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

ADVANTAGES

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

SIMPLIFIED SCHEMATIC



*C = 2 pF on LF157

ABSOLUTE MAXIMUM RATINGS

	LF155A/6A/7A	LF355A/6A/7A	LF155/6/7	LF255/6/7	LF355/6/7
Supply Voltage	±22V	±22V	±22V	±22V	±18V
Power Dissipation TO-99 (H package) (Note 1)	670 mW	500 mW	670 mW	570 mW	500 mW
Operating Temperature Range	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
$T_{j(MAX)}$	150°C	100°C	150°C	110°C	100°C
Differential Input Voltage	±40V	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C	300°C

DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155A/6A/7A			LF355A/6A/7A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		1	2		1	2	mV
		Over Temperature			2.5			2.3	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5		3	5	mV
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3,5)		3	10		3	10	pA
		$T_j \leqslant T_{HIGH}$			10			1	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3,5)		30	50		30	50	pA
		$T_J \leqslant T_{HIGH}$			25			5	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}		Ω
AV_{OL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$	50	200		50	200		V/mV
		$V_O = \pm10V$, $R_L = 2k$							
		Over Temperature	25			25			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$	±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1 −12		±11	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LF155A/355A			LF156A/356A			LF157A/357A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	LF155A/6A: $A_V = 1$, LF157A: $A_V = 5$	3	5		10	12		40	50		V/µs
GBW	Gain-Bandwidth Product			2.5		4	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		µs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$										
		f = 100 Hz		25			15			15		nV/$\sqrt{Hz}$
		f = 1000 Hz		20			12			12		nV/$\sqrt{Hz}$
i_n	Equivalent Input	f = 100 Hz		0.01			0.01			0.01		pA/$\sqrt{Hz}$
	Noise Current	f = 1000 Hz		0.01			0.01			0.01		pA/$\sqrt{Hz}$
C_{IN}	Input Capacitance			3			3			3		pF

DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155/6/7			LF255/6/7			LF355/6/7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25^\circ C$		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5			5		$\mu V/^\circ C$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		$\mu V/^\circ C$ per mV
I_{OS}	Input Offset Current	$T_j = 25^\circ C$, (Notes 3, 5)		3	20		3	20		3	50	pA
		$T_j \leq T_{HIGH}$			20			1			2	nA
I_B	Input Bias Current	$T_J = 25^\circ C$, (Notes 3,5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	$T_J = 25^\circ C$		10^{12}			10^{12}			10^{12}		Ω
AV_{OL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25^\circ C$	50	200		50	200		25	200		V/mV
		$V_O = \pm 10V$, $R_L = 2k$										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$	± 12	± 13		± 12	± 13		± 12	± 13		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	± 11	$+15.1$ -12		± 11	$+15.1$ -12		± 10	$+15.1$ -12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C$, $V_S = \pm 15V$

PARAMETER	LF155A/355A LF155/255		LF355		LF156A/356A LF156/256		LF356		LF157A/357A LF157/257		LF357		UNITS
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
Supply Current,	2	4	2	4	5	7	5	10	5	7	5	10	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C$, $V_S = \pm 15V$

SYMBOL	PARAMETER	CONDITIONS	LF155/LF255/ LF355	LF156/LF256	LF156/LF256/ LF356	LF157/LF257	LF157/LF257/ LF357	UNITS
			TYP	MIN	TYP	MIN	TYP	
SR	Slew Rate	LF155/6: $A_V = 1$, LF157: $A_V = 5$	5	7.5	12	30	50	V/μs
GBW	Gain-Bandwidth Product		2.5		5		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$						
		f = 100 Hz	25		15		15	nV/$\sqrt{Hz}$
		f = 1000 Hz	20		12		12	nV/$\sqrt{Hz}$
i_n	Equivalent Input	f = 100 Hz	0.01		0.01		0.01	pA/$\sqrt{Hz}$
	Current Noise	f = 1000 Hz	0.01		0.01		0.01	pA/$\sqrt{Hz}$
C_{IN}	Input Capacitance		3		3		3	pF

NOTES FOR ELECTRICAL CHARACTERISTICS

NOTE 1: The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.

NOTE 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

NOTE 3: These specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = +125°C$ unless otherwise stated for the LF155A/6A/7A and the LF155/6/7. For the LF255/6/7, these specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-25°C \leq T_A \leq +85°C$ and $T_{HIGH} = 85°C$ unless otherwise stated. For the LF355A/6A/7A, these specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $0°C \leq T_A \leq +70°C$ and $T_{HIGH} = +70°C$, and for the LF355/6/7 these specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

NOTE 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

NOTE 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta jA$ Pd where ΘjA is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

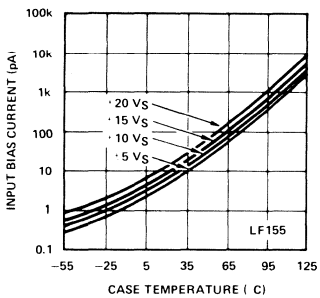
NOTE 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

NOTE 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit, page 9).

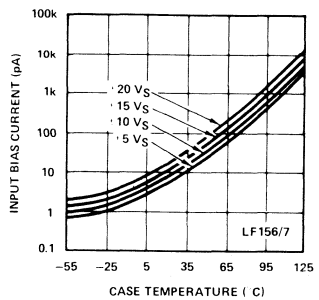
TYPICAL DC PERFORMANCE CHARACTERISTICS

Curves are for LF155, LF156 and LF157 unless otherwise specified.

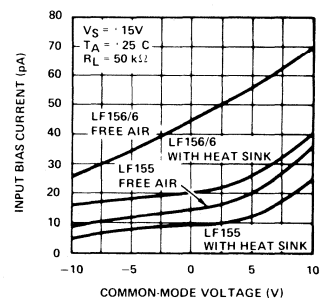
Input Bias Current



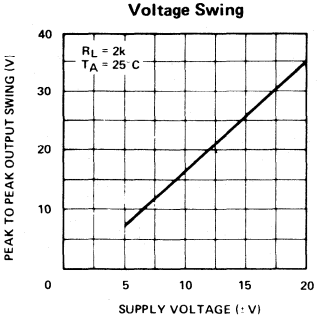
Input Bias Current



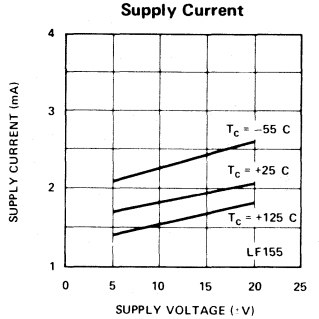
Input Bias Current



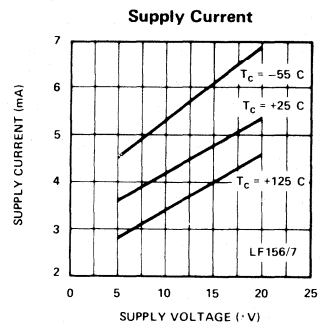
Voltage Swing



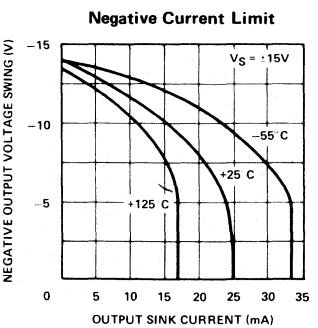
Supply Current



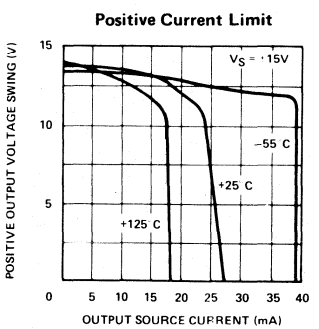
Supply Current



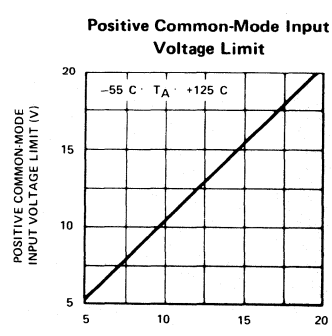
Negative Current Limit



Positive Current Limit

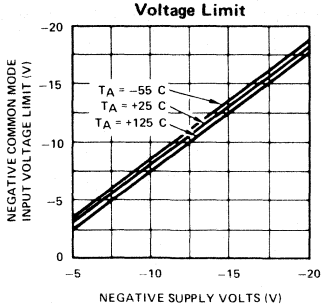


Positive Common-Mode Input Voltage Limit

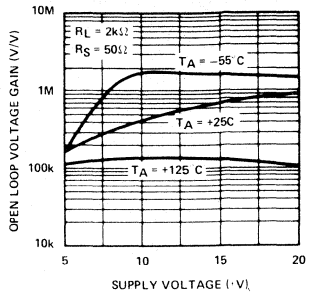


TYPICAL DC PERFORMANCE CHARACTERISTICS (CON'T)

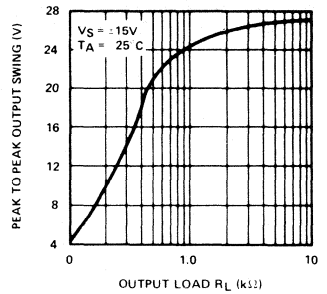
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain

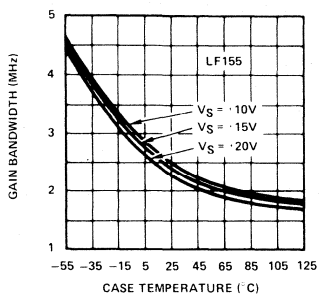


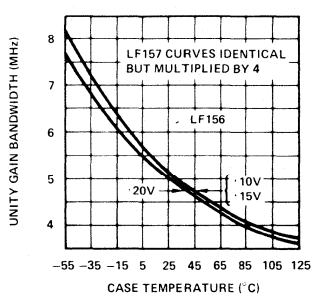
Output Voltage Swing



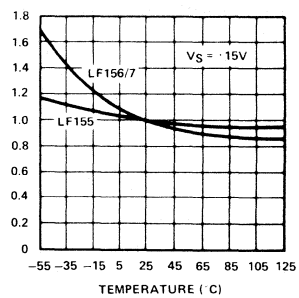
TYPICAL AC PERFORMANCE CHARACTERISTICS

Gain Bandwidth

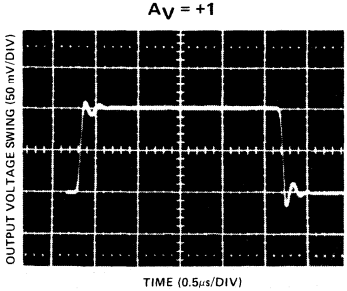




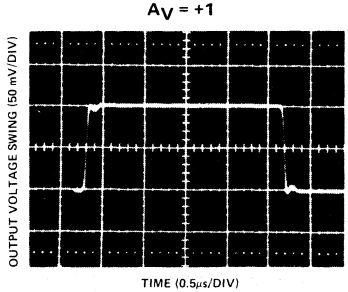
Normalized Slew Rate



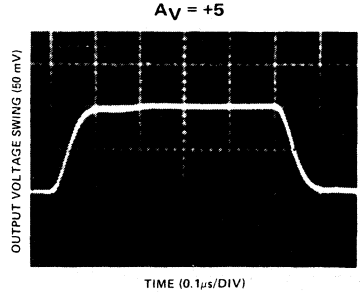
LF155 Small Signal Pulse Response, $A_V = +1$



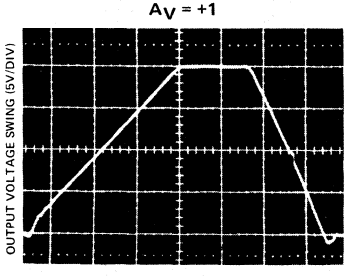
LF156 Small Signal Pulse Response, $A_V = +1$



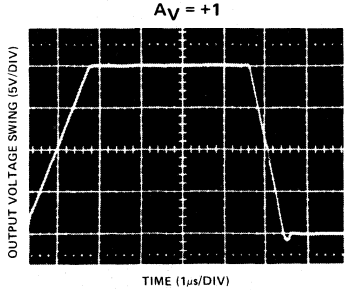
LF157 Small Signal Pulse Response, $A_V = +5$



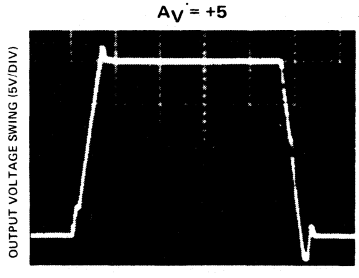
LF155 Large Signal Pulse Response, $A_V = +1$



LF156 Large Signal Pulse Response, $A_V = +1$

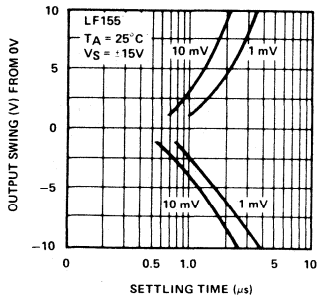


LF157 Large Signal Pulse Response, $A_V = +5$

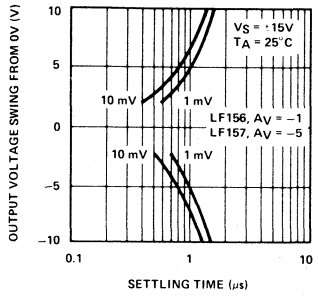


TYPICAL AC PERFORMANCE CHARACTERISTICS (CON'T)

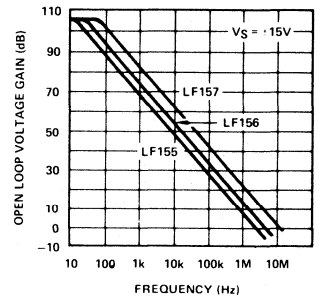
Inverter Settling Time



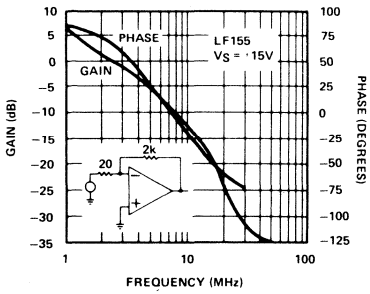
Inverter Settling Time



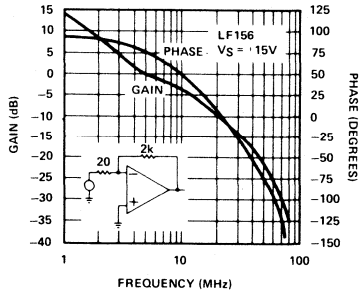
Open Loop Frequency Response



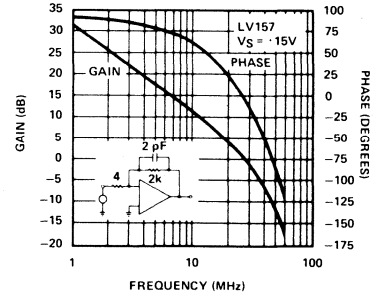
Bode Plot



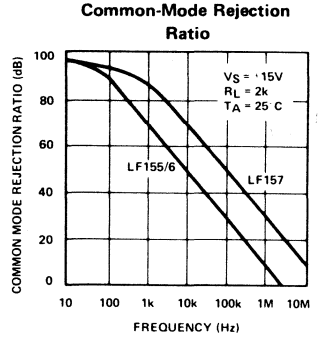
Bode Plot



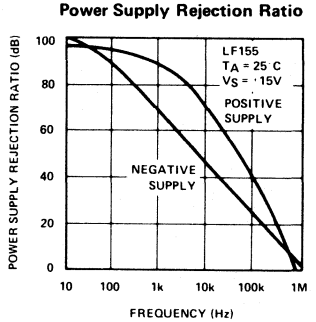
Bode Plot



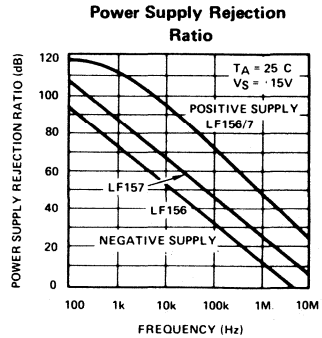
Common-Mode Rejection Ratio



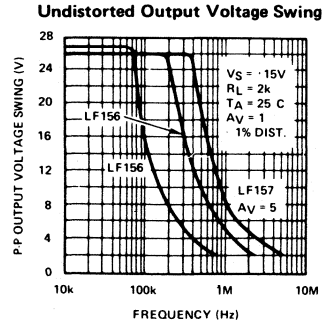
Power Supply Rejection Ratio



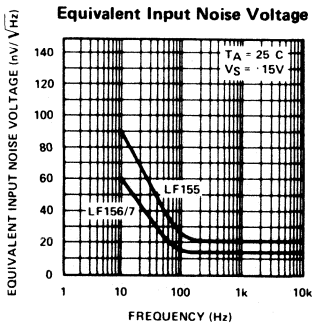
Power Supply Rejection Ratio



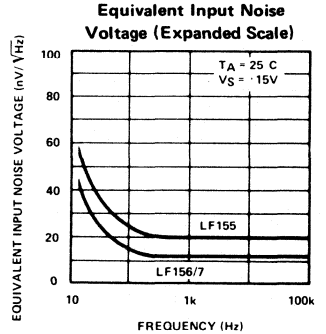
Undistorted Output Voltage Swing



Equivalent Input Noise Voltage

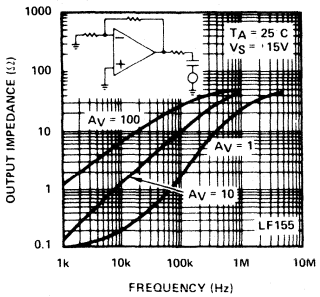


Equivalent Input Noise Voltage (Expanded Scale)

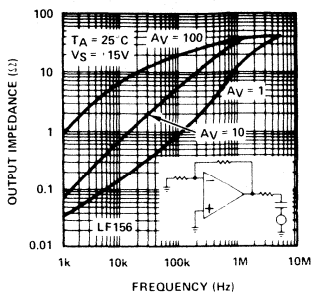


TYPICAL AC PERFORMANCE CHARACTERISTICS (CON'T)

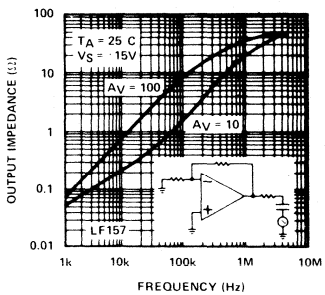
Output Impedance



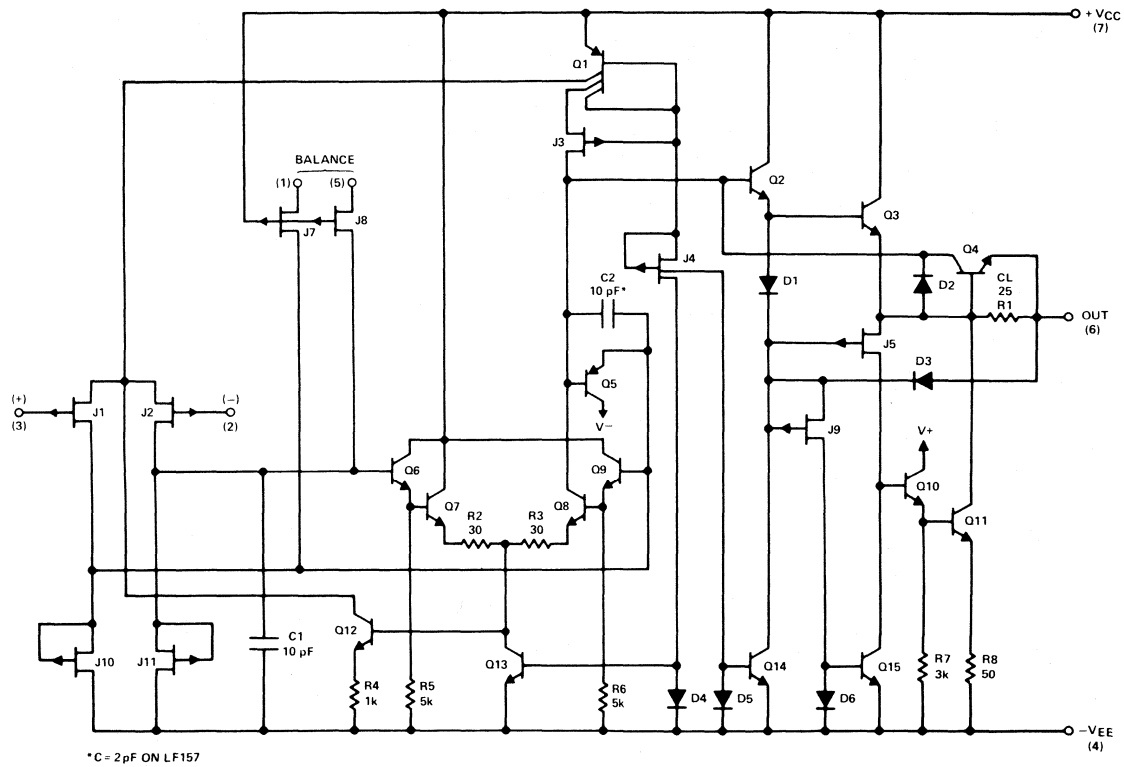
Output Impedance



Output Impedance



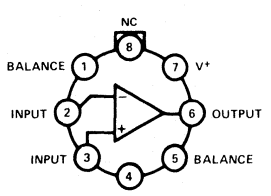
DETAILED SCHEMATIC



*C = 2 pF ON LF157

CONNECTION DIAGRAM

Metal Can Package



NOTE 4: PIN 4 CONNECTED TO CASE.

TOP VIEW

APPLICATION HINTS

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltage. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

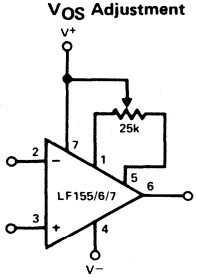
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

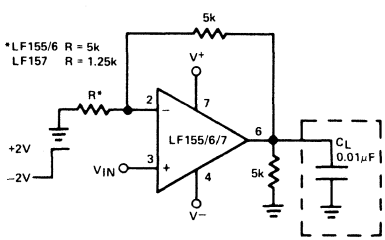
TYPICAL CIRCUIT CONNECTIONS

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5μV/°C/m of adjustment.
- Typical overall drift: 50V/°C ≅ (0.5μV/°C/mV of adj.)

Driving Capacitive Loads



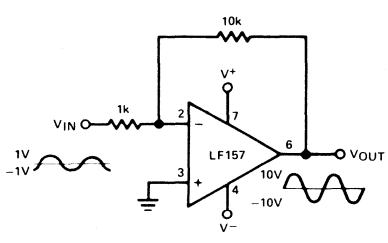
Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.

$C_{L\ MAX} \cong 0.01\mu F$.

Overshoot ≤ 20%.

Settling time (t_s) ≅ 5μs

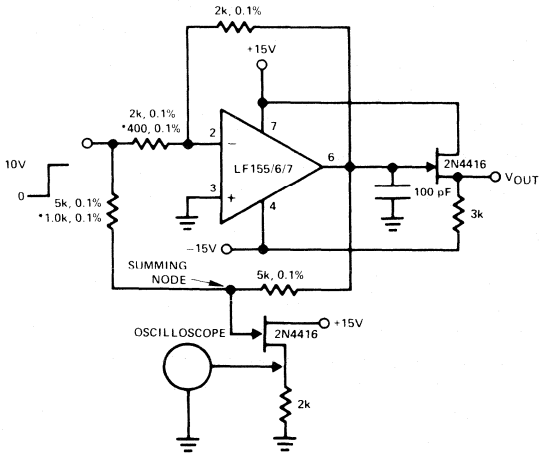
LF157. A Large Power BW Amplifier



For distortion < 1% and a 20 Vp-p V_{OUT} swing power bandwidth is: 500 kHz.

TYPICAL APPLICATIONS

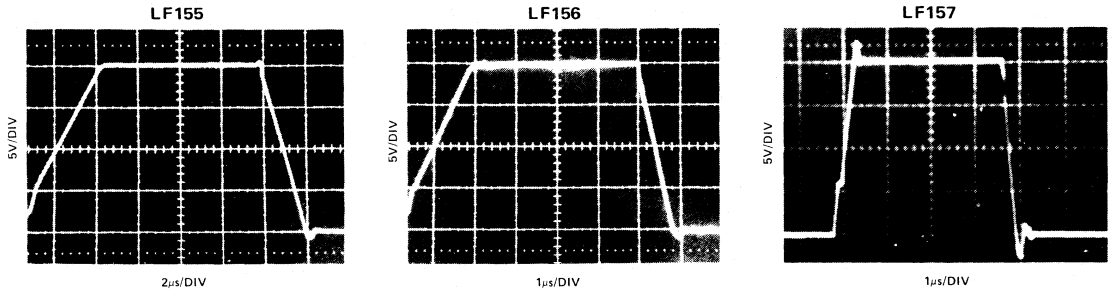
Settling Time Test Circuit



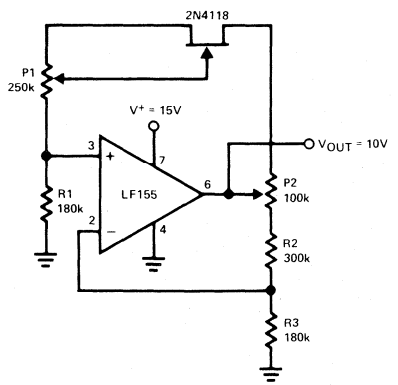
- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step

* $A_V = -5$ for LF157

Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)

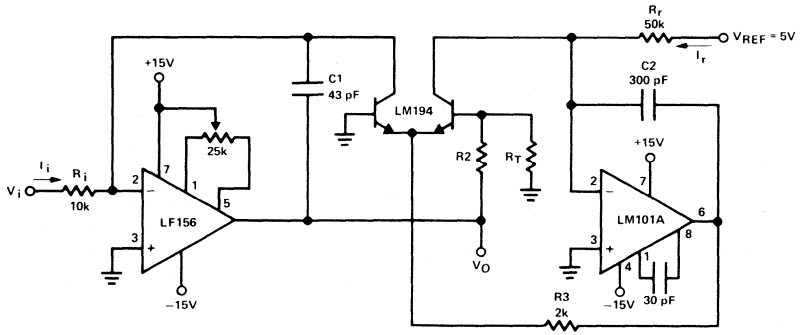


Low Drift Adjustable Voltage Reference



- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/°C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - Low I_B
  - Low drift
  - Low supply current

Fast Logarithmic Converter

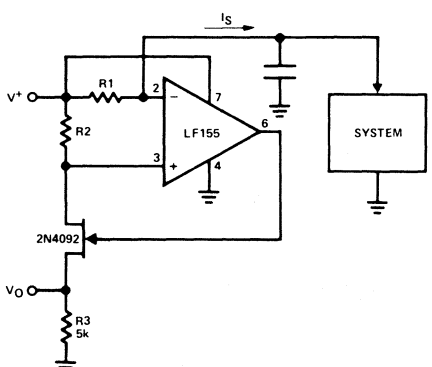


$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right]\frac{kT}{q} \quad \text{Ln } V_i \left[\frac{R_r}{V_{REF} R_i}\right] = \log V_i \frac{1}{R_i I_r}$$

R2 = 15.7k, R_T = 1k, 0.3%/°C (for temperature compensation)

- Dynamic range: 100μA ≤ I_i ≤ 1 mA (5 decades), $|V_O|$ = 1V/decade
- Transient response: 3μs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C.

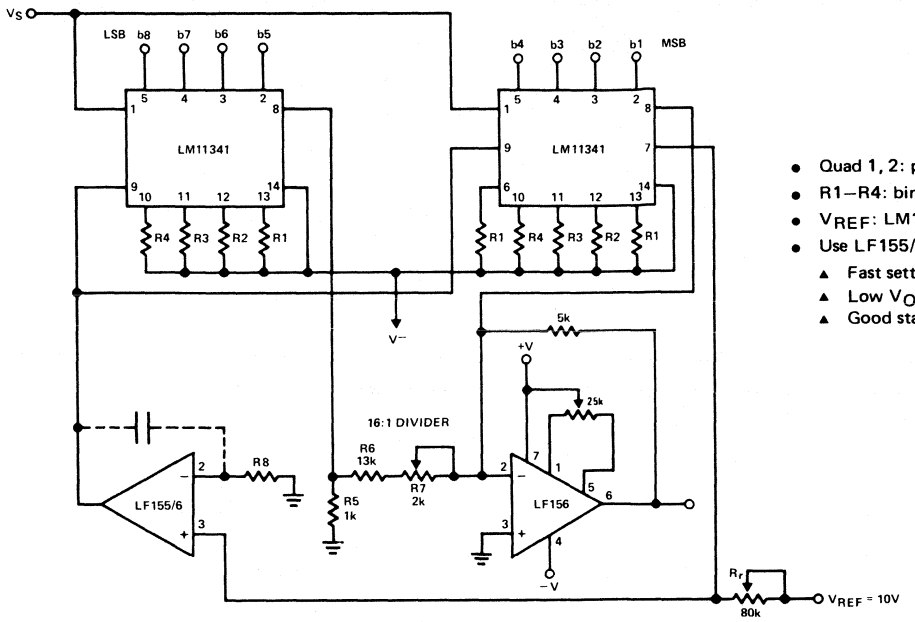
Precision Current Monitor



- $V_O = 5\frac{R1}{R2}$ (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common mode range to supply voltage
  - Low I_B
  - Low V_{OS}
  - Low supply current

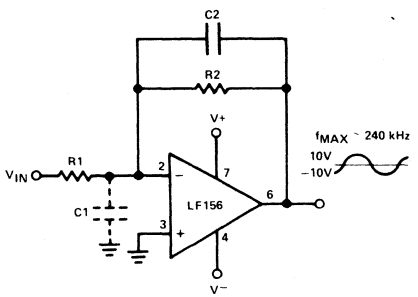
TYPICAL APPLICATIONS (CON'T)

LF156 as an Output Amplifier in a Fast 8-Bit DAC



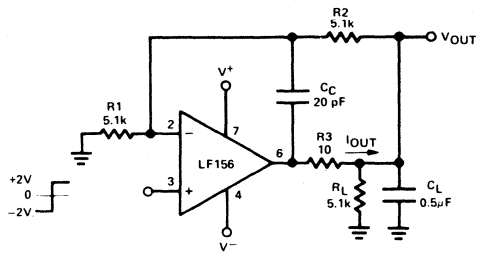
- Quad 1, 2: precision current switches
- R1–R4: binary ladder
- V_{REF}: LM113
- Use LF155/6 for
  - ▲ Fast settling time
  - ▲ Low V_{OS} drift
  - ▲ Good stability

Wide BW Low Noise, Low Drift Amplifier



- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 240\ kHz$
- Parasitic input capacitance C1 ≅ (3 pF for LF155, LF156, and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

Isolating Large Capacitive Loads



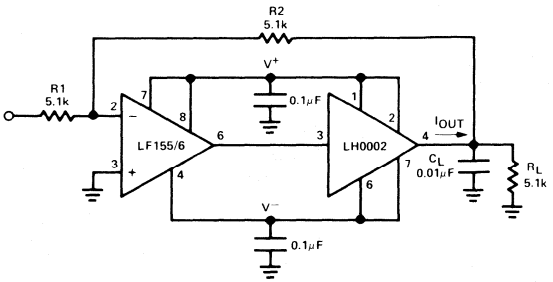
- Overshoot 6%
- t_s 10μs
- When driving large C_L the V_{OUT} slew rate determined by C_L and $I_{OUT\ MAX}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5} \quad V/\mu s = 0.04 V/\mu s$$

(with C_L shown)

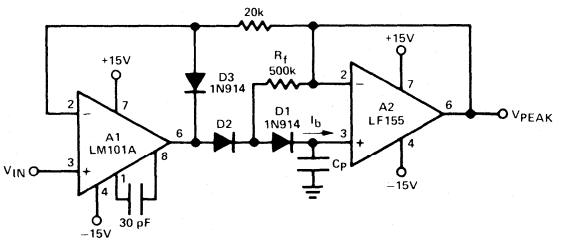
TYPICAL APPLICATIONS (CON'T)

Boosting the LF156 with a Current Amplifier



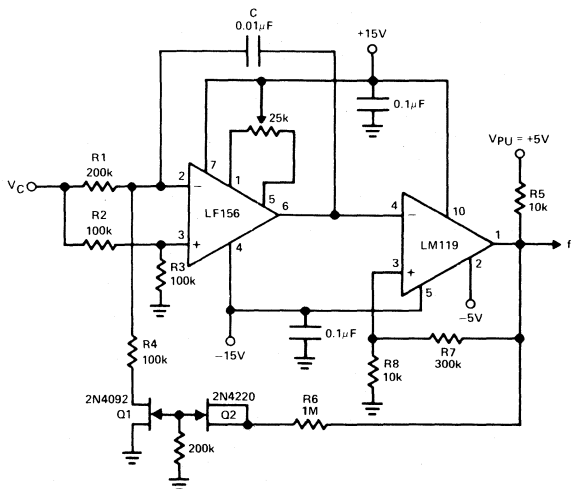
- $I_{OUT\ MAX} \cong 150$ mA (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = 15 V/\mu sec$ (with C_L shown)
- No additional phase shift added by the current amplifier

Low Drift Peak Detector



- By adding D1 and R_f, $V_{D1} = 0$ during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of C_P.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be $<< \frac{1}{2\pi R_f C_{D2}}$ where C_{D2} is the shunt capacitance of D2.

3 Decades VCO

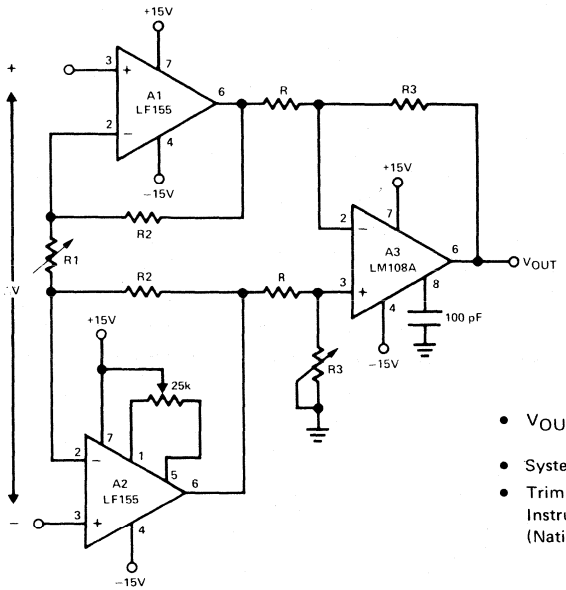


$$f = \frac{V_C\,(R8 + R7)}{[8\ V_{PU} R8 R1]\ C}, \quad 0 \leq V_C \leq 30V,\ 10\ Hz \leq f \leq 10\ kHz$$

R1, R4 matched. Linearity 0.1% over 2 decades.

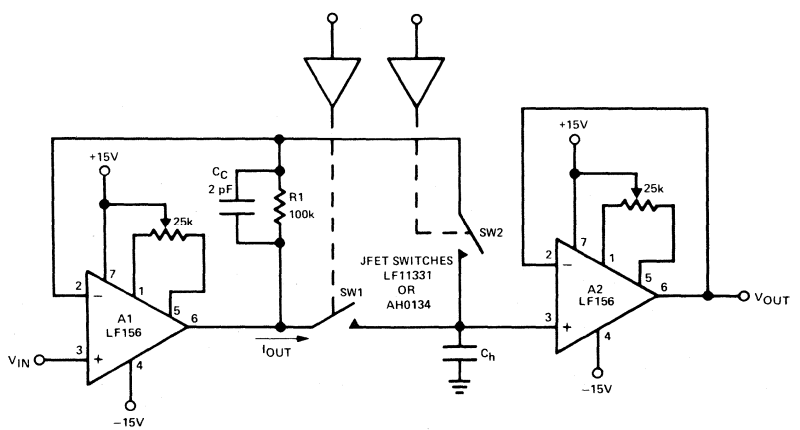
TYPICAL APPLICATIONS (CON'T)

High Impedance, Low Drift Instrumentation Amplifier



- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right]$ $\Delta V, V^- + 2V \leq V_{IN}$ Common-Mode $\leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier Resistor array RA201 (National Semiconductor) recommended

Fast Sample and Hold



- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time, T_A, estimated by:

$$T_A \cong \left[\frac{2R_{ON} \cdot V_{IN} \cdot C_h}{Sr}\right]^{1/2}$$ provided that:

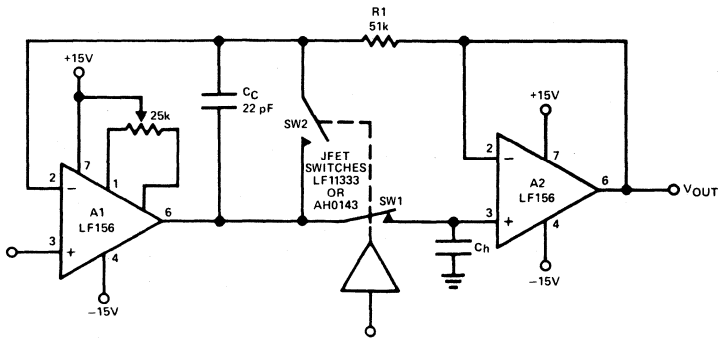
$$V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT\ MAX}}$$, R_{ON} is of SW1

If inequality not satisfied: $T_A \cong \frac{V_{IN} C_h}{20\ mA}$

- LF156 develops full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

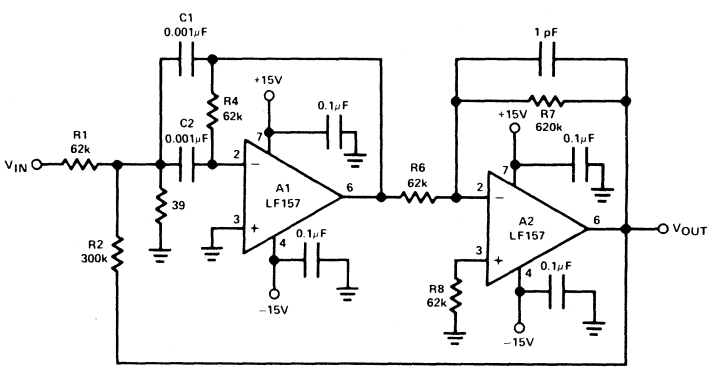
TYPICAL APPLICATIONS (CON'T)

High Accuracy Sample and Hold



- By closing the loop through A2 the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - ▲ Fast settling time
  - ▲ Low V_{OS}

High Q Band Pass Filter



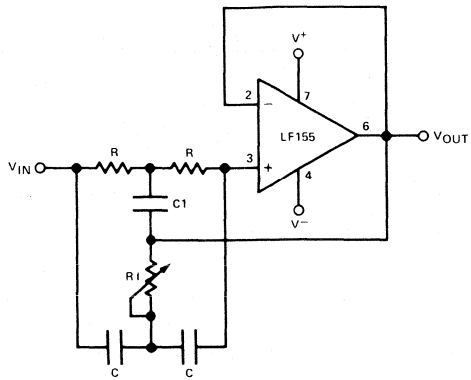
- By adding positive feedback (R2) Q increases to 40
- f_{BP} = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300μs

TYPICAL APPLICATIONS (CON'T)

High Q Notch Filter



- 2R1 = R = 10MΩ
  2C = C1 = 300 pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - ▲ Low I_B
  - ▲ Low supply current

DEFINITION OF TERMS

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

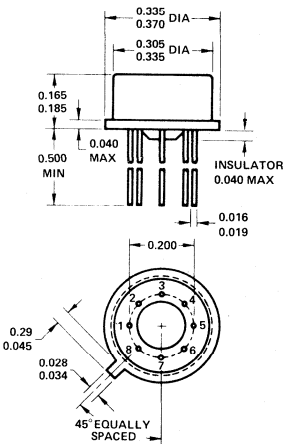
Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Power Supply Rejection Ratio: The ratio of the change in input offset voltage to the change in power supply voltage producing it. The typical curves in this sheet show values for each supply independently changed. The electrical specification, however, is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Settling Time: The time required for the error between input and output to settle to within a specified limit after an input is applied to the test circuit shown in typical applications.

PACKAGE DIMENSIONS

TO-99 METAL CAN PACKAGE (H)



ORDER NUMBER:

LF155AH	LF157H	LF356AH
LF156AH	LF255H	LF357AH
LF157AH	LF256H	LF355H
LF155H	LF257H	LF356H
LF156H	LF355AH	LF357H

LM148/LM248/LM348 QUAD 741 OP AMPS
LM149/LM249/LM349 WIDE BAND DECOMPENSATED ($A_{V(MIN)}$=5)

LM148, LM149

FEATURES

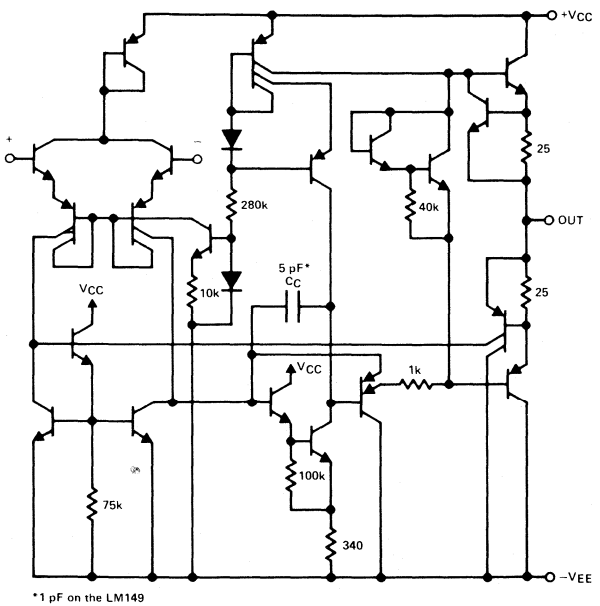
- 741 op amp operating characteristics
- Low supply current drain — 0.6 mA/Amplifier
- Class AB output stage—no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage — 1 mV
- Low input offset current — 4 nA
- Low input bias current — 30 nA
- Gain bandwidth product
  - LM148 (unity gain) — 1.0 MHz
  - LM149 ($A_V \geqslant 5$) — 4 MHz
- High degree of isolation between amplifiers — 120 dB
- Overload protection for inputs and outputs

GENERAL DESCRIPTION

The LM148 series is a true quad 741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling. The LM149 series has the same features as the LM148 plus a gain bandwidth product of 4 MHz at a gain of 5 or greater.

The LM148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

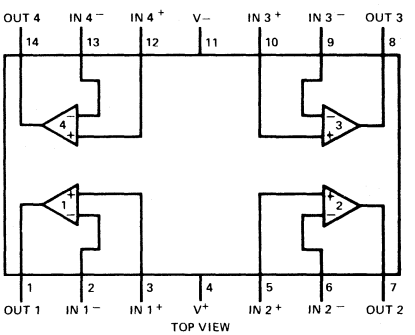
EQUIVALENT SCHEMATIC



*1 pF on the LM149

CONNECTION DIAGRAM

DUAL-IN-LINE AND FLAT PACKAGE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

	LM148/LM149	LM248/LM249	LM348/LM349
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage	±44V	±36V	±36V
Input Voltage	±22V	±18V	±18V
Output Short Circuit Duration (Note 1)	Continuous	Continuous	Continuous
Power Dissipation (P_d at 25°C) and			
Thermal Resistance (θ_{jA}), (Note 2)			
Molded DIP (N) P_d	–	–	500 mW
θ_{jA}	–	–	150°C/W
Cavity DIP (D) (J) P_d	900 mW	900 mW	100°C/W
θ_{jA}	100°C/W	100°C/W	100°C/W
Flat Pack (F) P_d	675 mW	–	–
θ_{jA}	185°C/W	–	–
Maximum Junction Temperature (T_{jMAX})	150°C	110°C	100°C
Operating Temperature Range	$-55°C \leqslant T_A \leqslant +125°C$	$-25°C \leqslant T_A \leqslant +85°C$	$0°C \leqslant T_A \leqslant +70°C$
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C	300°C	300°C

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	LM148/LM149			LM248/LM249			LM348/LM349			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S \leqslant 10\ k\Omega$		1.0	5.0		1.0	6.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		4	25		4	50		4	50	nA
Input Bias Current	$T_A = 25°C$		30	100		30	200		30	200	nA
Input Resistance	$T_A = 25°C$	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers	$T_A = 25°C$, $V_S = \pm 15V$		2.4	3.6		2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$	50	160		25	160		25	160		V/mV
	$V_{OUT} = \pm 10V$, $R_L \geqslant 2\ k\Omega$										
Amplifier to Amplifier	$T_A = 25°C$, f = 1 Hz to 20 kHz		−120			−120			−120		dB
Coupling	(Input Referred) See Crosstalk Test										
	Circuit										
Small Signal Bandwidth	$T_A = 25°C$ LM148 series		1.0			1.0			1.0		MHz
	$T_A = 25°C$ LM149 series		4.0			4.0			4.0		MHz
Phase Margin	$T_A = 25°C$ LM148 series ($A_V = 1$)		60			60			60		degrees
	$T_A = 25°C$ LM149 series ($A_V = 5$)		60			60			60		degrees
Slew Rate	$T_A = 25°C$ LM148 series ($A_V = 1$)		0.5			0.5			0.5		V/μs
	$T_A = 25°C$ LM149 series ($A_V = 5$)		2.0			2.0			2.0		V/μs
Output Short Circuit Current	$T_A = 25°C$		25			25			25		mA
Input Offset Voltage	$R_S \leqslant 10\ k\Omega$			6.0			7.5			7.5	mV
Input Offset Current				75			125			100	nA
Input Bias Current				325			500			400	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$,	25			15			15			V/mV
	$R_L > 2\ k\Omega$										
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$,	±12	±13		±12	±13		±12	±13		V
	$R_L = 2\ k\Omega$	±10	±12		±10	±12		±10	±12		V
Input Voltage Range	$V_S = \pm 15V$	±12			±12			±12			V
Common-Mode Rejection	$R_S \leqslant 10\ k\Omega$	70	90		70	90		70	90		dB
Ratio											
Supply Voltage Rejection	$R_S \leqslant 10\ k\Omega$	77	96		77	96		77	96		dB

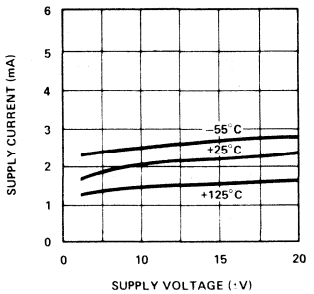
Note 1. Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

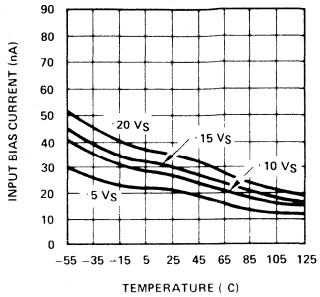
Note 3: These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leqslant T_A \leqslant T_H$) unless otherwise noted.

TYPICAL PERFORMANCE CHARACTERISTICS

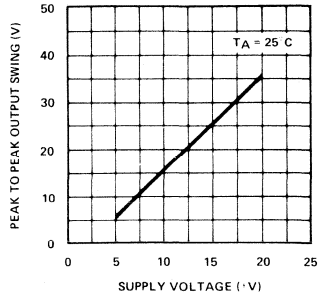
Supply Current



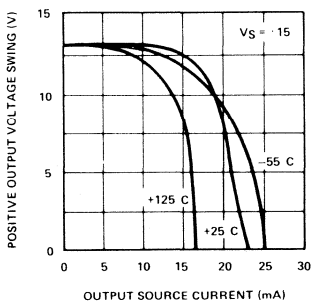
Input Bias Current



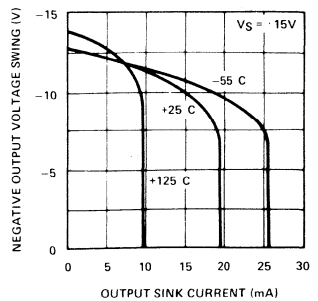
Voltage Swing



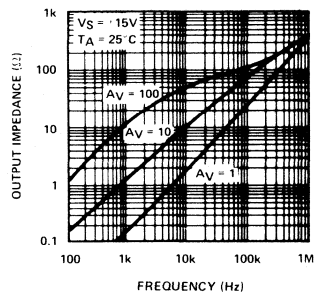
Positive Current Limit



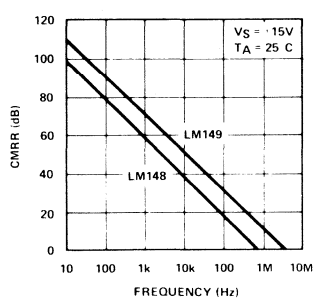
Negative Current Limit



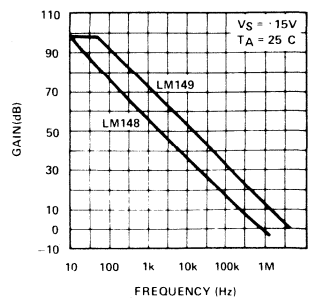
Output Impedance



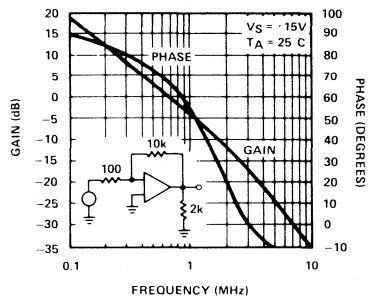
Common-Mode Rejection Ratio



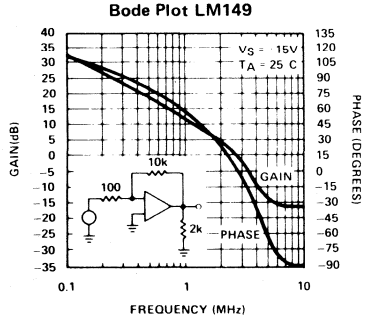
Open-Loop Frequency Response



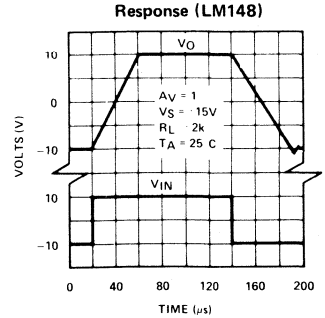
Bode Plot LM148



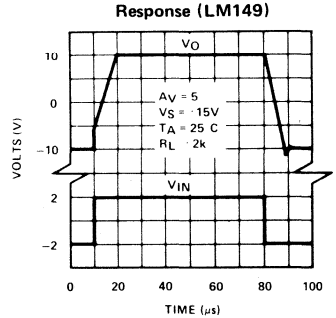
Bode Plot LM149



Large Signal Pulse Response (LM148)

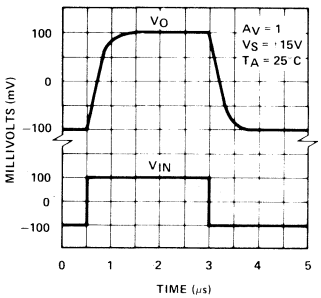


Large Signal Pulse Response (LM149)

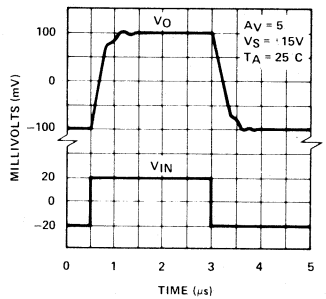


TYPICAL PERFORMANCE CHARACTERISTICS (CON'T)

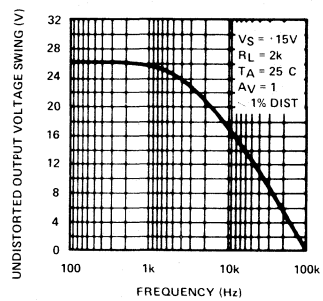
Small Signal Pulse Response (LM148)



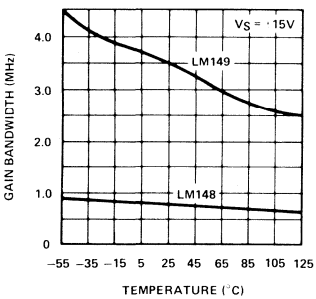
Small Signal Pulse Response (LM149)



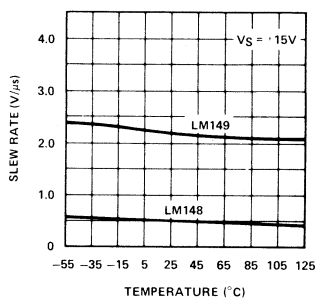
Undistorted Output Voltage Swing



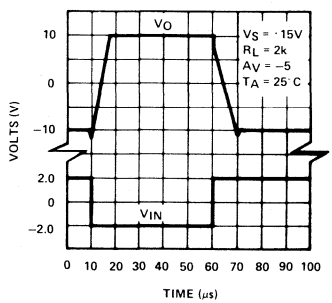
Gain Bandwidth



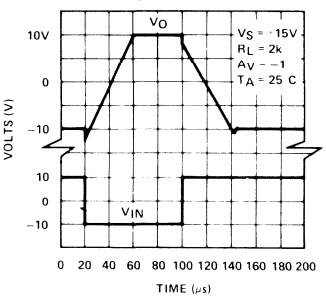
Slew Rate



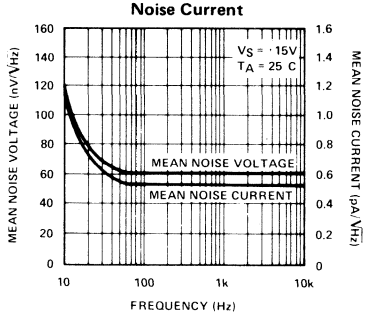
Inverting Large Signal Pulse Response (LM149)



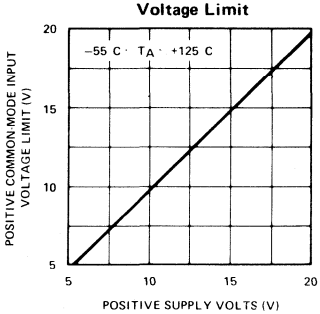
Inverting Large Signal Pulse Response (LM148)



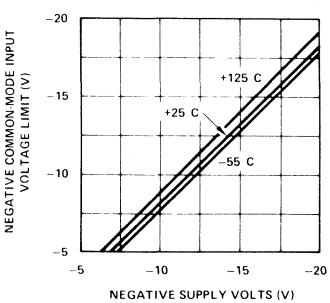
Input Noise Voltage and Noise Current



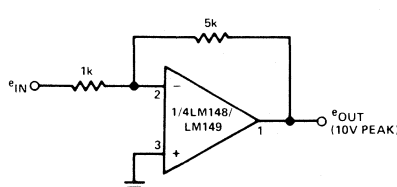
Positive Common-Mode Input Voltage Limit

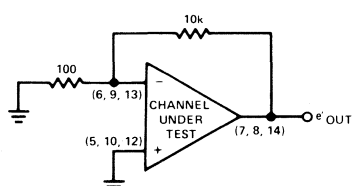


Negative Common-Mode Input Voltage Limit



CROSS TALK TEST CIRCUITS





$$\text{Crosstalk} = -20 \log \frac{e'_{OUT}}{101 \times e_{OUT}} \quad (dB)$$

$V_S = \pm 15V$

APPLICATION HINTS

The LM148 series are quad low power 741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familiar, easy to use operating characteristics of the 741 op amp. In those applications where 741 op amps have been employed, the LM148 series op amps can be employed directly with no change in circuit performance.

The LM149 series has the same characteristics as the LM148 except it has been decompensated to provide a wider bandwidth. As a result the part requires a minimum gain of 5 for stability.

The package pin-outs are such that the inverting input of each amplifier is adjacent to its output. In addition, the amplifier outputs are located in the corners of the package which simplifies PC board layout and minimizes package related capacitive coupling between amplifiers.

The input characteristics of these amplifiers allow differential input voltages which can exceed the supply voltages. In addition, if either of the input voltages is within the operating common-mode range, the phase of the output remains correct. If the negative limit of the operating common-mode range is exceeded at both inputs, the output voltage will be positive. For input voltages which greatly exceed the maximum supply voltages, either differentially or common-mode, resistors should be placed in series with the inputs to limit the current.

Like the LM741, these amplifiers can easily drive a 100 pF capacitive load through the entire dynamic output voltage and current range. However, if very large capacitive loads must be driven by a non-inverting unity gain amplifier, a resistor should be placed between the output (and feedback connection) and the capacitance to reduce the phase shift resulting from the capacitive loading.

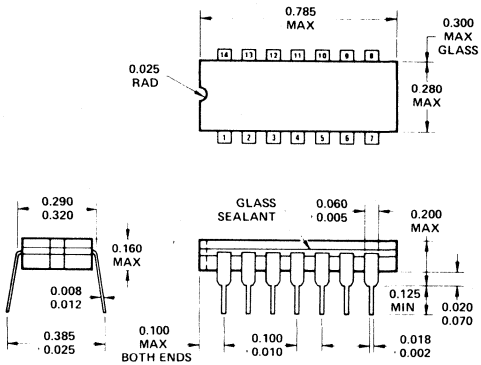
The output current of each amplifier in the package is limited. Short circuits from an output to either ground or the power supplies will not destroy the unit. However, if multiple output shorts occur simultaneously, the time duration should be short to prevent the unit from being destroyed as a result of excessive power dissipation in the IC chip.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole which capacitance from the input to ground creates.

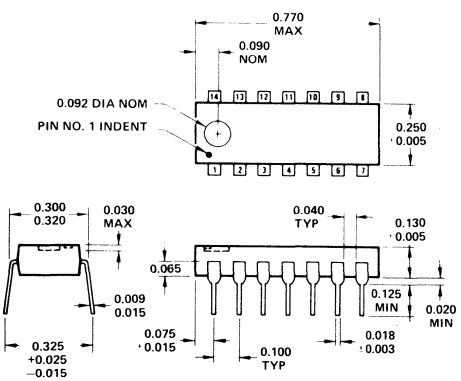
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

PACKAGE DIMENSIONS

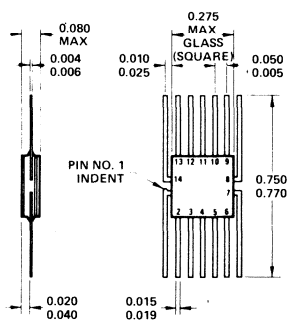
Cavity Dual-In Line Package
Order Number LM148, LM149, LM248
LM249, LM348, or LM349



Molded Dual-In-Line Package (N)
Order Number LM348N or LM349N



Flat Package (F)
Order Number LM148F or LM149F



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